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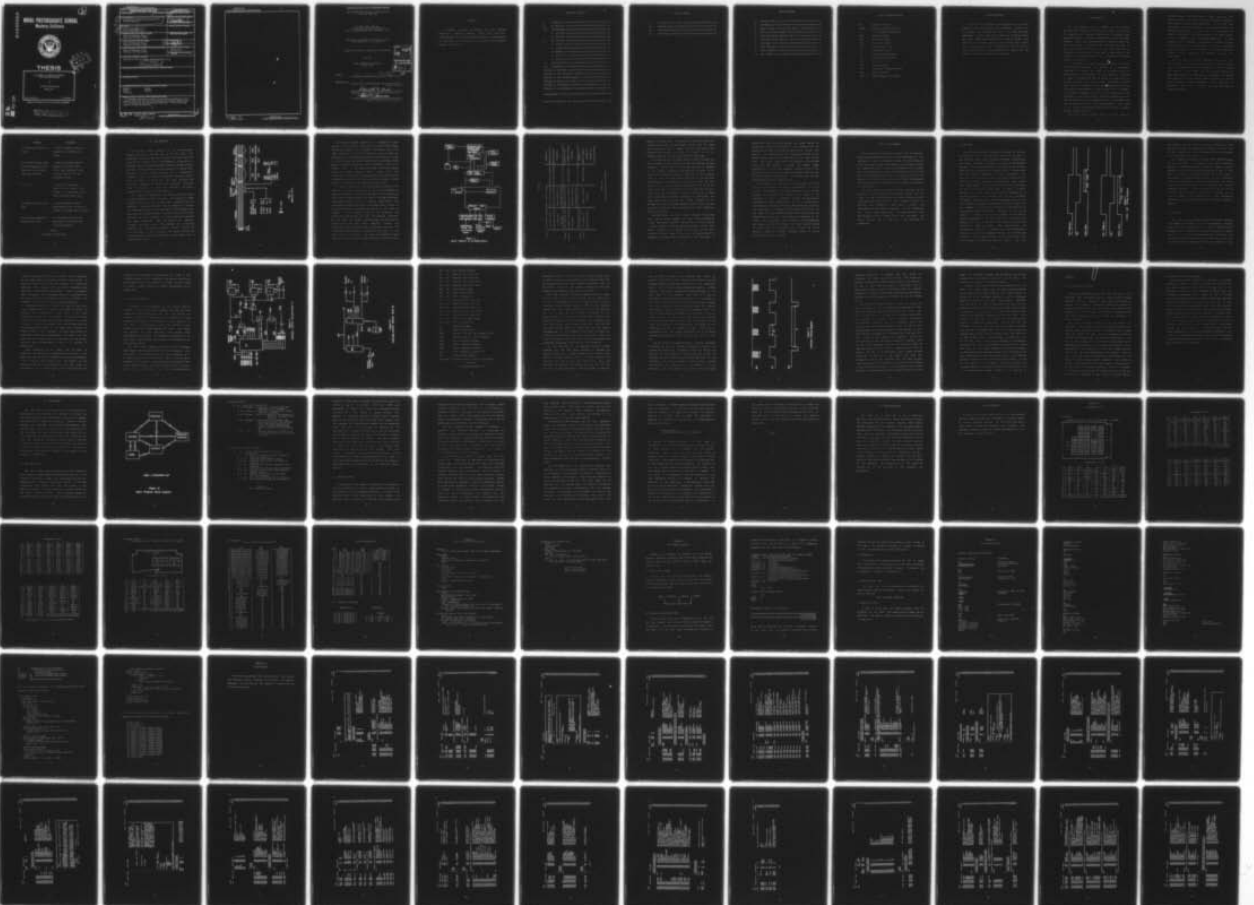
AN INTERACTIVE COMPUTER INTERFACE WITH A DIGITAL RECEIVER.(U)

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## THESIS

AN INTERACTIVE COMPUTER INTERFACE  
WITH A DIGITAL RECEIVER

by

William Glenn Borries

March 1977

Thesis Advisor:

S. Jauregui

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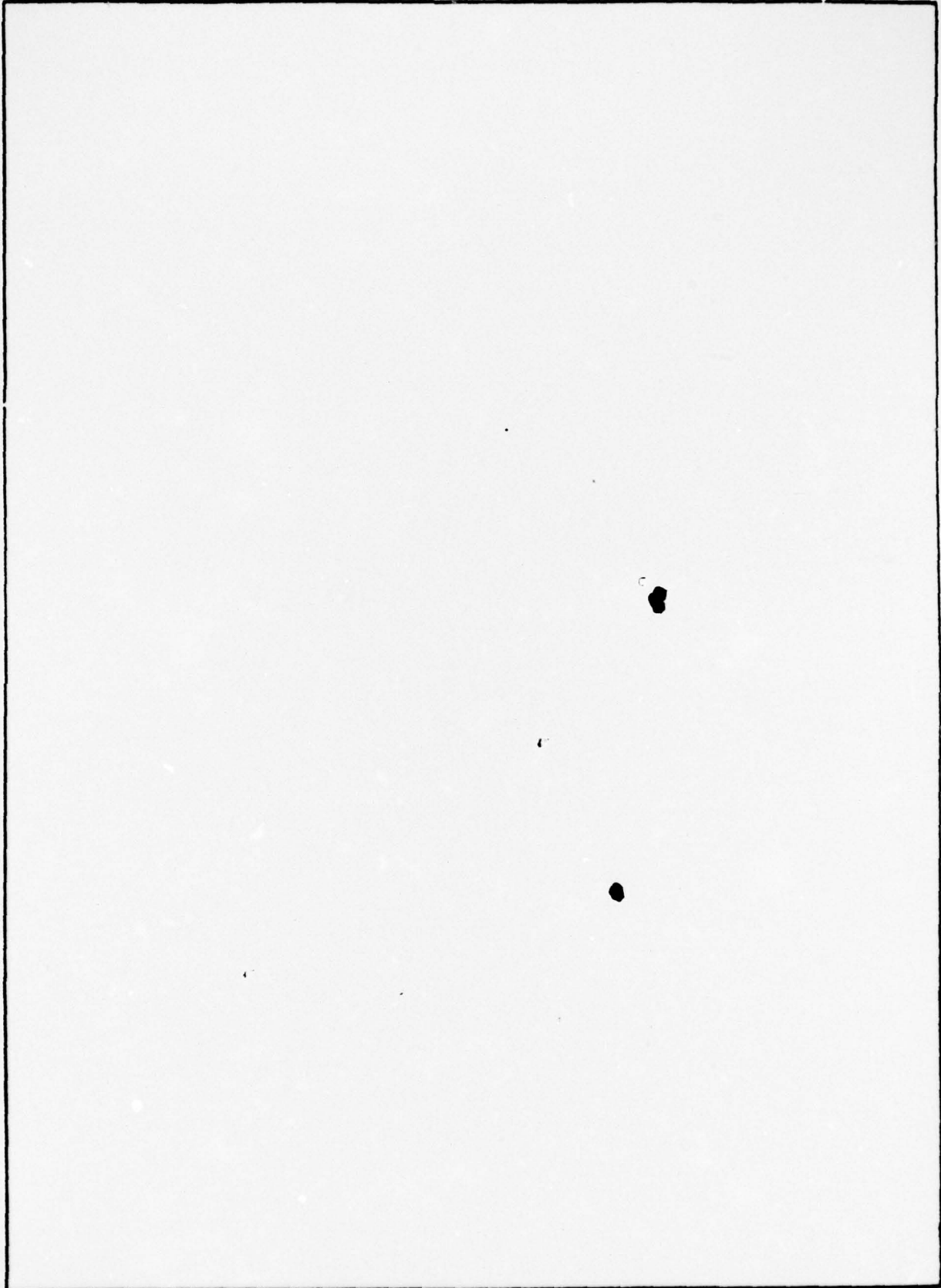
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An Interactive Computer Interface with  
a Digital Receiver

by

William Glenn Borries  
Lieutenant, United States Navy  
B.S., United States Naval Academy, 1970

Submitted in partial fulfillment of the  
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL  
March, 1977

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# ABSTRACT

A computer interface to connect both the Applied Technology Airborne Computer (ATAC) and the KIM-1 Microprocessor to a Watkins Johnson digitally tuned receiver was designed and constructed. The existing ATAC computer program was modified.



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## LIST OF ABBREVIATIONS

A/D	Analog to Digital
ASCII	American Standard Code for Information Interchange
Baud	Bits per second
D/A	Digital to Analog
high	TTL logic 1 (+5v)
I/O	Input and/or Output
IC	Integrated Circuit
IF	Intermediate Frequency
ISB	Intermediate Sideband
low	TTL logic 0 (0v)
LSB	Lower Sideband
TTL	Transistor Transistor Logic
USB	Upper Sideband
BFO	Beat Frequency Oscillator

## ACKNOWLEDGEMENTS

I would like to express my deep appreciation to Carole Hickey who wrote the initial ATAC programs. Without her Main System the programming that I did would have been unbearable. I would also like to thank the following people who have helped along the way: LT. Al May, Al Gilkes, Greg Ramos, LT. Bill Hickey, Bob Glaz, Dave Blonden, Dean Hayes, and Virginia Ward. Most importantly, I want to thank my wife, Cathy, for all the encouragement and advice she has given me during the writing of this thesis.



## I. INTRODUCTION

For many decades man has dreamed of the day when machines could relieve him of much of his work. In this era of computers and advanced technology, this dream is now becoming a reality. Connecting computers to other machines, however, is not just a simple matter of running a wire from one to the other. In order for the computer to be able to use its "thinking" ability, it must have some way to translate its signals into a form that is recognized by the machine it is controlling. This is where the interface becomes all important.

An interface is a piece of equipment placed in the data path between two devices. Its purpose is to rearrange, translate, or change the speed of this data to meet the needs of one or both devices. In other cases the interface is used to convert data from an analog to digital (A/D) or digital to analog (D/A) form, or both. Interfaces of either type range in complexity from a few integrated circuits to the use of microprocessors. Most, however, fall in between. This thesis discusses the design and construction of an interface in this middle class. Here, the computers are the Applied Technology Airborne Computer (ATAC) minicomputer and the MOS Technology Inc.'s 6801 microprocessor. Their goal is to program and process outputs from a digitally tunable Watkins Johnson WJ-8888.

The two computer systems arrive at their goal by



different means. The ATAC uses a closed loop with the operator (Figure 1a) while the KIM-1 excludes the operator while executing its program (Figure 1b). In the ATAC loop the operator actively controls all communication between the computer and receiver. In this way it is possible to display information from the receiver on the video display at any time except during a scan (see Chapter V). It also provides quick reference to the data to be sent, the data last sent, and latest received data. This was invaluable during debugging. From the terminal it is also possible to adjust available parameters as necessary to meet any requirement.

The KIM-1 does not directly exchange digital words with the receiver, but rather exchanges digital data for analog data. This does not provide a feedback loop that includes the operator. Once begun, the KIM-1 program selects and sends data words to the receiver and processes the analog data received until the program comes to an end or is halted by the operator. Direct information is not available to determine when or if a digital word has been sent or received correctly.

Problems encountered during the design and construction of the interface and their solutions are shown in Table I. In this instance signal level compatability was not a problem because the I/O from the receiver, the interface, and the two computers were all TTL logic levels and, therefore, matched. It is believed that these problems are a typical list that may be encountered when interfacing.

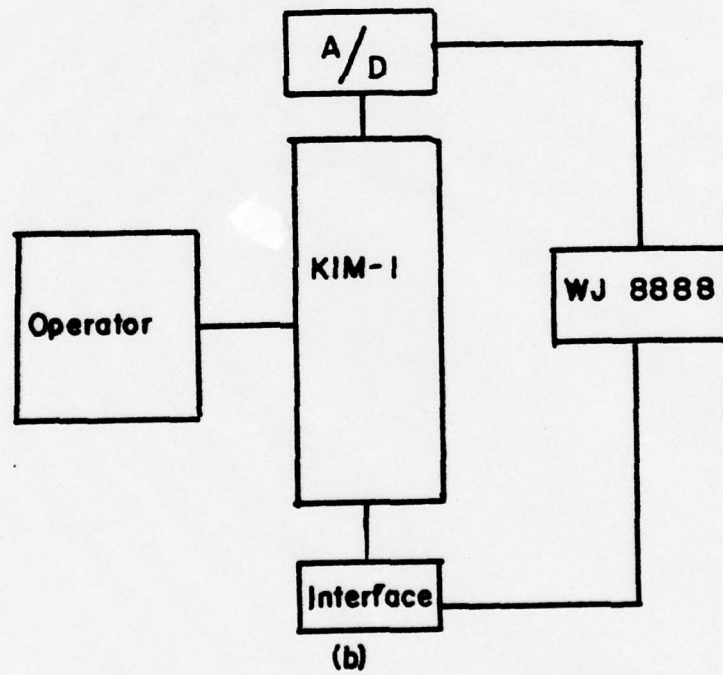
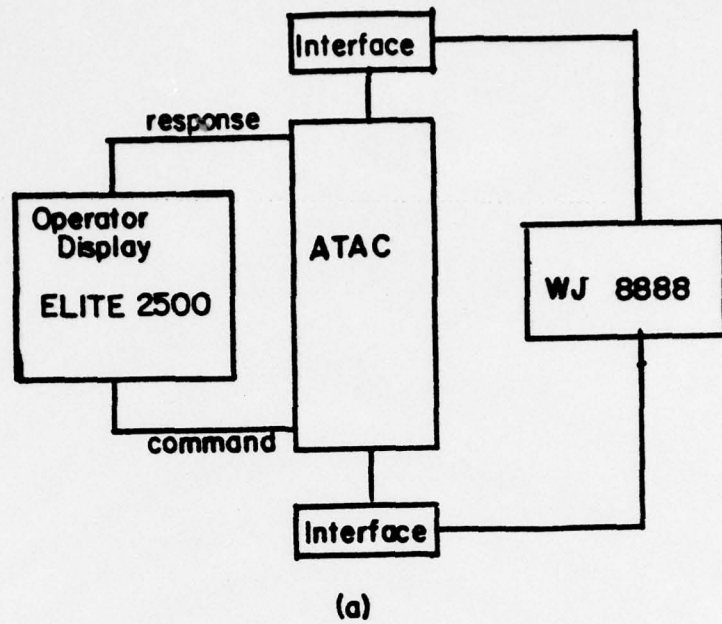


Figure 1  
Computer Control

## PROBLEM

## SOLUTION

1. Noise on the ATAC I/O lines.

1. Use of Schottky circuits reduced or eliminated the noise.

2. Different clock rates of the computers and the receiver, and different data word lengths.

2. ATAC; converted parallel outputs into serial form. KIM-1; used interrupt lines to slave the KIM-1 to the receiver's clock.

3. Timing

3. Identified receiver periods by the Monitor Clock output. This provided a pulse which signaled stable data.

4. Inputting data to the ATAC.

4. Open collector buffers were used to sink the required current for proper data transfer.

5. Switching between the ATAC and the KIM-1.

5. Multiplexers and buffers were used to switch between the two computers.

Table I  
Problems and Solutions



## II. THE RECEIVER

The Watkins Johnson WJ-8888 (WJ) is an HF receiver designed for use in the 550 KHz to 30 MHz band. Its advantages include the ability to detect and output both the AM and FM IF signals while simultaneously maintaining a separate output of eight selectable detection modes. Options available to the operator include different IF bandwidths, variable RF gain, squelch control, and a tuneable BFO frequency. The WJ is digitally controlled and uses a 64-bit word as shown in Figure 2. This word contains the information necessary to transfer the frequency, detection mode, IF bandwidth, RF gain, BFO frequency, and signal strength both internally and externally.

All inputs and outputs from the receiver are controlled by the synchronous, remote I/O board. This board is a gated transfer point for all digital data exchanged with the receiver. A number of control lines are needed to provide the necessary demands on the receiver. Three balanced input pairs and four balanced output line pairs, plus a ground are provided for this purpose. All three inputs are required for remote operation. They are address (or enable), trigger, and data input. The address pair is the most important for it serves as the master "on-off" switch for the remainder of the I/O pairs. The outputs furnish the required clocks (command and monitor), output data, and a local/remote status.



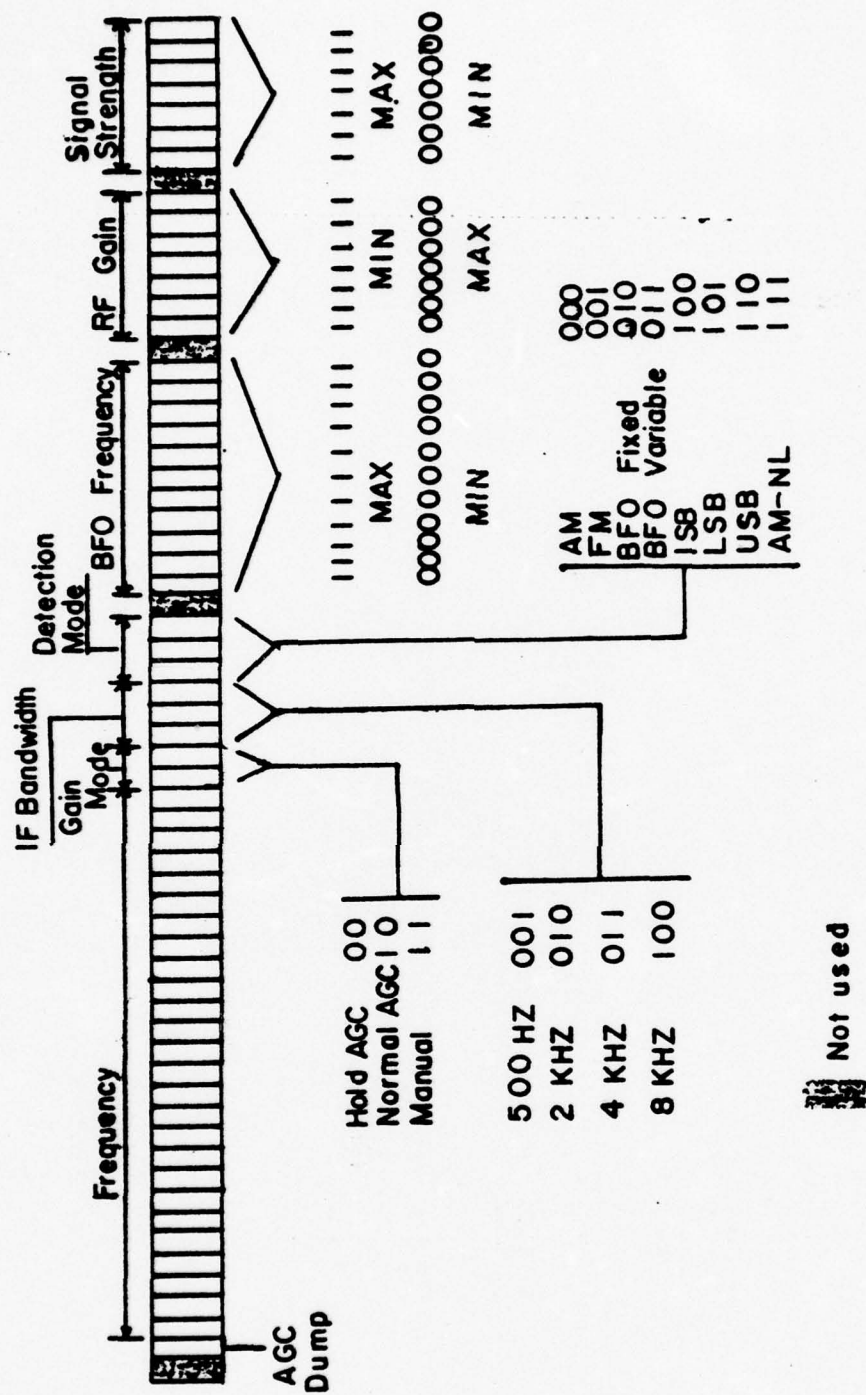


Figure 2  
Receiver's Word

The Watkins Johnson operates on a sequential cycle divided into four equal periods and six identifiable modes. The periods regulate the different operations while the modes ascertain the origin of the data. Table II shows the interaction of the periods and modes of the receiver. Three of the six modes are memory read and write functions; these cannot be remotely controlled and, therefore, are of no concern here. Of the remaining three, two are the remote active and remote passive modes. These allow the introduction of externally generated data and prevent manual intervention during all but one of the four periods. Manual control is available in the remaining mode, local.

In order to manage the data word movement correctly, the receiver utilizes a common bus or data node arrangement as shown in Figure 3. This simplifies operation by forcing all data words to pass through this node in the same direction, regardless of their origin or desired destination. The multiplexer controls the input to the data node. Control of the multiplexer and, therefore, the origin of the data is managed by the internal modes of the receiver. The objective of period one is to load the receiver register. In the local and remote passive modes, the data word is shifted from the front panel register, through the multiplexer and data node, into the receiver register. The difference between these two modes is in the action of the data prior to shifting. The local mode updates the data word from the front panel storage registers during the early

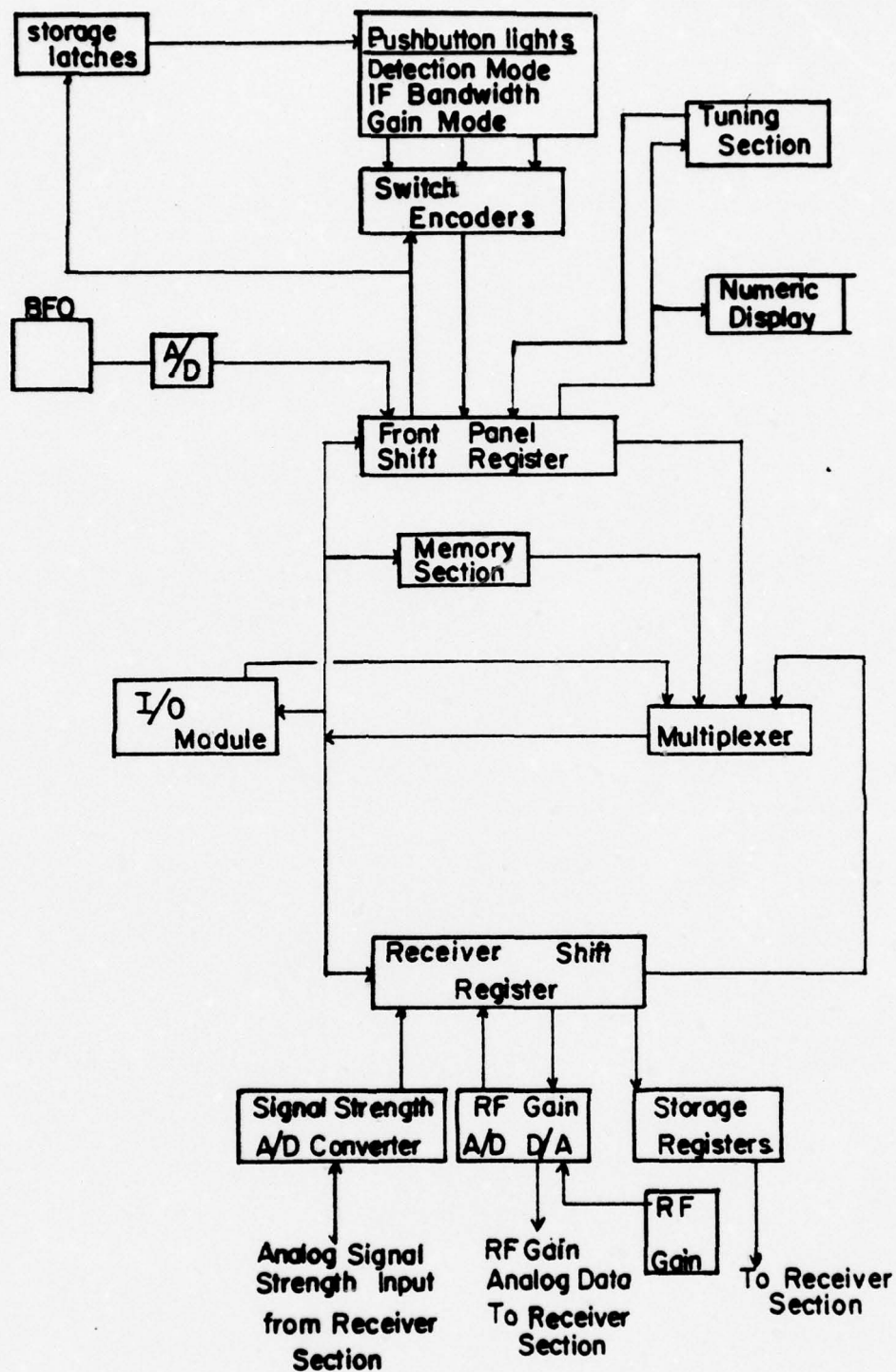


Figure 3  
Block Diagram of the Digital Section

Period

	1	2	3	4
Local	Load Front Panel Reg from Front Panel/word shifted to Receiver Register	Load Rcvr Storage Reg/ Signl Strength and RF gain updated /word shifted to FrontPanel Register	Display updated no words shifted	Change to Remote Active or Remote Passive possible
Remote Passive	Word shifted from FrontPanel Register to Receiver	Update only Sig Str /Load Kcvr Storage Reg/word shifted to FrontPanel Reg.	Same as Local	Change to Lcl or Remote Active possible
Remote Active	Word shifted from I/O module to Receiver Register	Same as Remote Passive	Same as Local	Change to Remote Passive automatic. Change to Local possible

Table II  
Receiver Modes and Periods



portion of period one. This action is inhibited during the remote passive mode. In the remote active mode the data word originates from a remote device, is shifted by the command clock through the remote I/O board, on to the receiver register via the multiplexer and data node.

The first part of the second period is spent loading the data shifted during period one into the receiver storage registers. During this time the signal strength is updated in the receiver register regardless of the mode. The RF gain A/D-D/A converter functions according to the selected mode. In the local mode the RF gain bits in the data word are replaced by A/D conversion of the front panel RF gain control knob. The two remote modes reverse this action and load the RF gain D/A converter with this data from the word. After this is completed, the word is shifted in all modes out of the receiver register, through the multiplexer and data node, and into the front panel register. If the address line from the remote device is active high, the data word and the monitor clock are available on their respective output line pairs.

Periods three and four inhibit movement of the data word. Period three updates the front panel pushbutton lights and numeric display. Period four is the only period in which changes in receiver mode are allowed. During this period changes from a remote mode to local, or from local directly to remote passive can only be accomplished by depressing the appropriate pushbutton on the front panel. A



change from local and remote passive to remote active is automatically done by the remote I/O board whenever both the address and trigger line pairs are active high during this period. The remote active mode immediately reverts to the remote passive mode at the beginning of the next period four. The total cycle time of the receiver is 10.24 msec (2.56 msec per period). In order to change modes successfully, it may be necessary either to hold in the pushbutton or to hold the trigger and address lines high for up to 7.68 msec (three periods). This ensures that the mode change demand occurs in period four.

All outputs are available from connectors J1, and J6 through J10 located on the back of the receiver. J1 is the digital I/O connector. The other connectors are all analog outputs. J6 is a 455 KHz IF signal of at least 20 KHz bandwidth. AM and FM detector monitors are provided at connectors J7 and J9 respectively. J8 is a predetection, 455 KHz center frequency IF output whose bandwidth is set by the front panel. A balanced and unbalanced line audio and both upper and lower sideband outputs are available from the appropriate pins at J10. The balanced line operates at all times. The unbalanced line is operable unless headphones are plugged into the front panel. The lower sideband output is active when the receiver is in either ISB or LSB detection modes, and the upper sideband output is active during ISB, USB, and CW modes.

### III. THE COMPUTERS

After studying the inputs and outputs from the receiver, three choices were available for further development of the interface. It could be designed to pass the clock pulses on to the interrupt lines of the computer and, therefore, match the computer's timing to that of the receiver. Or, a buffer could be constructed to input the data serially at the clock rate of the computer and output it at the clock rate of the receiver. The third choice, also a buffering arrangement, could exchange data in parallel to the computer and serially to the receiver.

The chief factor influencing the design decision was the availability and distribution of computer control and I/O lines. For the first computer, the primary objective was to investigate the feasibility of both remotely tuning the receiver and accepting a data word in return. The requirements for the second computer, the MOS Technology Inc. KIM-1, were less strict. Its objective was to tune the receiver digitally through use of the interface. Its input, however, was to come from a A/D converter for processing.

## A. THE ATAC

The ATAC was originally designed to provide EW service to aircraft. Built to do real-time analysis of signals, it has very short cycle times, optional microcode programming, and double precision arithmetic as part of the standard package. All this, combined with its large instruction set, makes the ATAC a versatile and powerful tool. Although data could be transferred serially by proper programming, the ability of the ATAC to both input and output sixteen bits in parallel on the PIO (parallel input/output) lines proved more advantageous. Any one of the ATAC's sixteen registers can input or output from these lines. In order to properly transfer this data, the PIO bus must be augmented by an address provided by the sixteen bits of the "extended" Arithmetic Register (XAR). Another necessary output is one that informs the external device when the ATAC is ready for the transfer. On the ATAC this function is provided by the Input/Output Demand (IOD) line. Referring to the timing diagram in Figure 4, an input command is initiated by placing an address on the XAR lines and following this address with a low on the IOD. This signifies that the ATAC register is ready for data. After approximately one microsecond, the IOD is placed high and the address is removed. During this microsecond the data for the ATAC must be stable. For an output command, the XAR and the PIO lines first present the address and data for output. When they

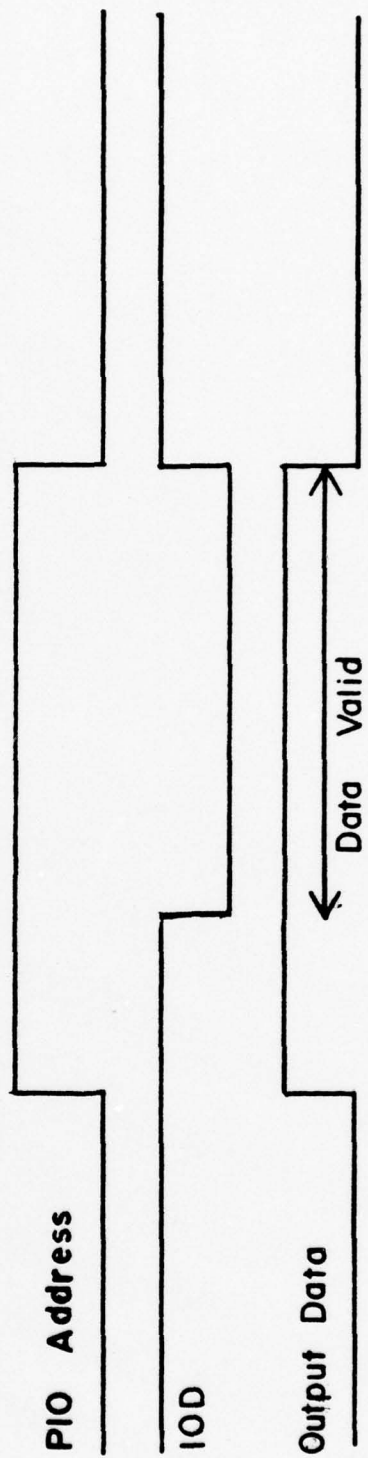
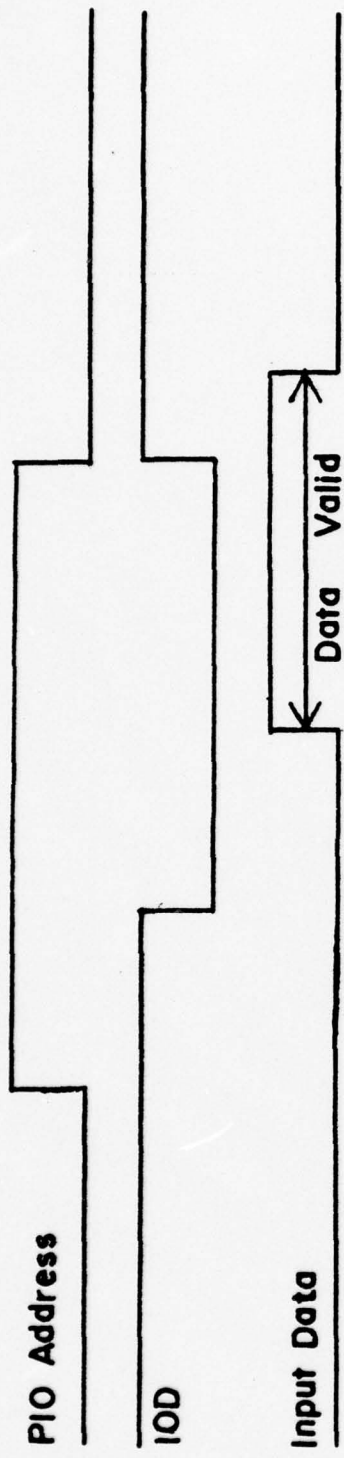


Figure 4  
ATAC I/O Timing Diagram



are stable, the IOD line is set low. The data is then available for about a microsecond, as before. The IOD line is then placed high and the address and data are removed from their respective lines.

For operator interaction a serial ASCII, RS232 I/O port is also available. A Datamedia Elite 2500 television terminal is connected here to provide the operator with the necessary control and programming capability for use of the ATAC. By proper programming and use of the XAR lines, it was possible to translate each command for the interface. Using a demultiplexer on the interface board, four of the five available XAR addresses were separated into sixteen separate commands. One of the remaining lines and the IOD line were used as strobes to identify the receiver and to signify stable data (Chapter III). This arrangement provided both the adequate isolation and flexible operation desired.

## B. THE KIM-1

The KIM-1 is at the other end of the computer spectrum with respect to the ATAC. It is a microprocessor designed around the MOS Technology Inc. series MCS6500 Central Processor Unit. Complete on a single printed circuit board, the KIM-1 is simple to operate and easy to program. While its cycle time is slower than that of the ATAC, it is still much faster than the receiver and more than adequate to meet

the requirements. Since the input data came from converted analog data supplied from the receiver's FM IF output (J9) and an external A/D converter, the design for this portion of the interface was simpler.<sup>1</sup>

-----  
<sup>1</sup>For a more detailed discussion of the KIM-1, its objectives, programs, and operating procedures, see Signal Acquisition and Sampling Using a Microprocessor, by LT. D. Rosenberger.

#### IV. THE INTERFACE

The interface was initially designed solely for the ATAC. A means of converting four ATAC words into one receiver word was needed first, in order to test the program, the computer, and the receiver together. The simplest and cheapest way to accomplish this conversion and still fully utilize the capabilities of the ATAC was to build a 64-bit register using eight parallel-in, serial-out, eight-bit shift registers. A control section was also necessary to properly handle this data. The ATAC XAR addresses were decoded by this control section to provide the load commands for the registers and to signal the receiver to input the word.

The next step in construction was also simple in theory. Since the computer uses the PIO lines for input as well as output, what was needed was a connection which would not interfere with the section already built. The ICs chosen to isolate the two sections are called Tri-State. These ICs have a "no output" state in addition to the normal high and low of TTL circuits. They could not, however, sink or supply enough current to drive the computer PIO bus. A solution was found by following these ICs with open collector buffers. Not only did they provide the necessary amplification, they did not degrade the isolation performance of the Tri-States. This second section also had

a 64-bit register built from the smaller shift registers. In this case, though, they were serial-in, parallel-out. In order to remove the word from the register in sixteen-bit sections, the outputs from the shift registers were connected to four-to-one multiplexers. These multiplexers were Tri-State. With the proper control it was possible to shift the word from the receiver into this register, and transfer it to the PIO bus in the correct sequence.

Increased complexity in the control section came with this implementation. A method was needed to prevent the computer from transferring a word until it had been completely shifted into the register. The period two clock output from the receiver was used as a reference to provide a pulse to inform the computer when shifting was complete. This pulse was positioned in the same time interval as period three of the receiver. The additional benefit of identifying period four was obtained. This meant that the output for the tripper line to the receiver could be shorter and still meet the requirement to occur in a portion of period four.

After completion of the testing for the ATAC, an interface was designed and constructed for the KIM-1. This design was very simple to implement, since all the necessary timing circuits were already built and tested. The two computers were kept from interfering with each other by installation of a manual switch. This switch controls the



address of a multiplexer that separates the lines in the interface common to both computers. The control section was wire-wrapped, rather than placed on a printed circuit board to provide greater flexibility, easier maintenance, and to reduce cost.

#### A. THE CONTROL SECTION

The heart of the interface is the control section (Figures 5 and 6). The main purpose of this section is to decode and route commands from the ATAC and provide the necessary circuits to interface with the receiver. It also contains the circuits for the operation of the receiver by the KIM-1. The receiver's outputs are driven by line drivers which provide complementary TTL levels. The inputs are applied to line receivers which accept these complementary TTL levels. The interface, therefore, had to use these same receivers and drivers to be compatible with the Watkins Johnson.

The SPST switch mounted on the front of the interface case selects the computer controlling the receiver. With the switch in the ATAC position, a high is placed on pin 1 of IC-JJ and pins 1 and 10 of IC-MM. IC-JJ is now set up to transfer the following: the address and data outputs to the line drivers on IC-LL, the trigger command to pin 2 of IC-Z, and a low in line CCK7. The CCK7 line completes the



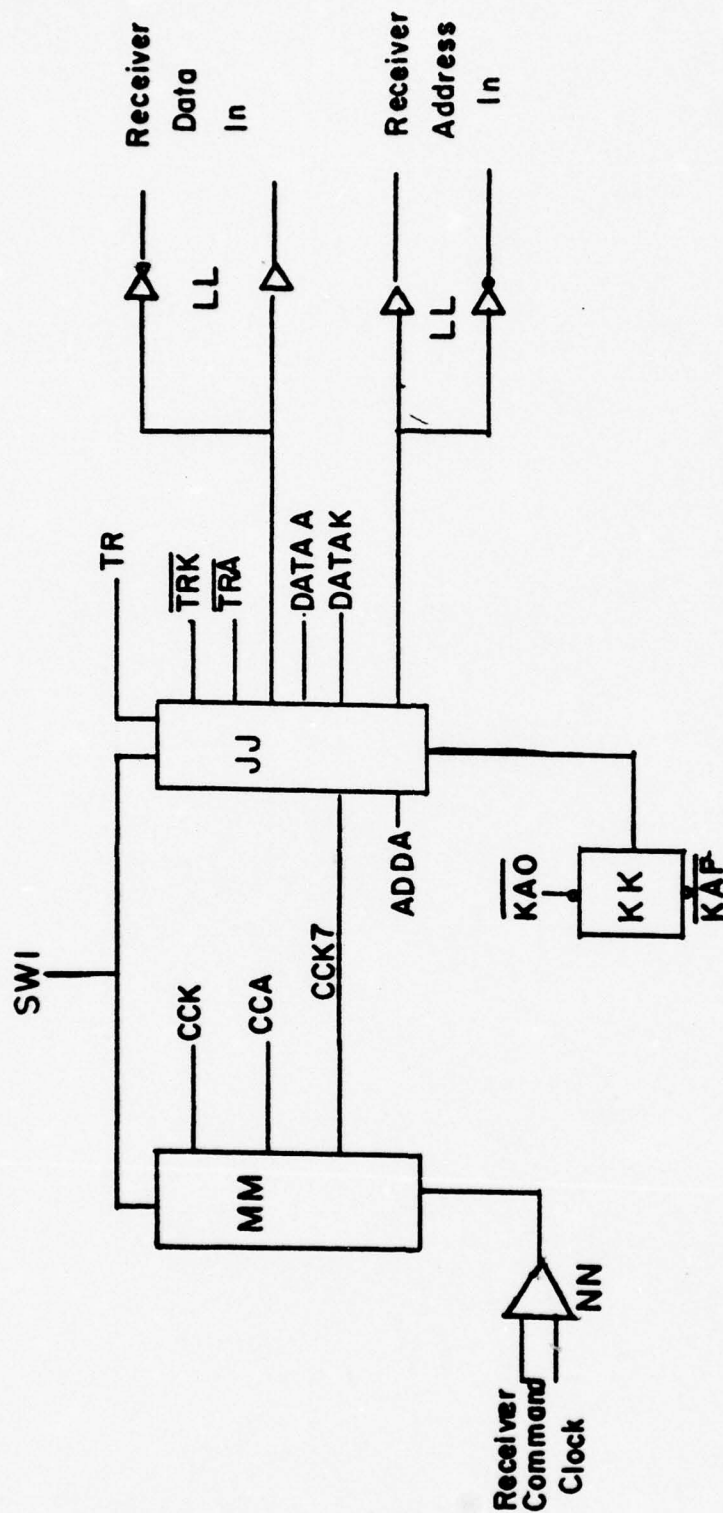


Figure 6  
Interface Control Section (Part 2)

TRA	[0]	ATAC Trigger Command
DIA	[1]	Receiver input word one
DIB	[2]	Receiver input word two
DIC	[3]	Receiver input word three
DID	[4]	Receiver input word four
DSP	[5]	Stop Monitor Clock
DST	[6]	Start Monitor Clock
ADD	[7]	ATAC - Address on
DOA	[8]	Receiver output word one
DOR	[9]	Receiver output word two
DOR	[9]	Receiver output word two
DOC	[10]	Receiver output word three
DOD	[11]	Receiver output word four
RDY	[12]	Read D11 for ready signal
ADF	[15]	ATAC - Address off
TR		Receiver trigger
CLK		KIM-1 Command Clock
CLK7		Control Line for KIM-1 Command Clock
CCA		Command Clock for ATAC interface
ADDA		ATAC - Receiver Address
KADD		KIM-1 - Receiver Address
KAO		KIM-1 - Receiver Address On
KAF		KIM-1 - Receiver Address Off
TRK		KIM-1 Trigger Command
(Numbers in brackets refer to ATAC XAR commands)		

Table III  
Interface Command List



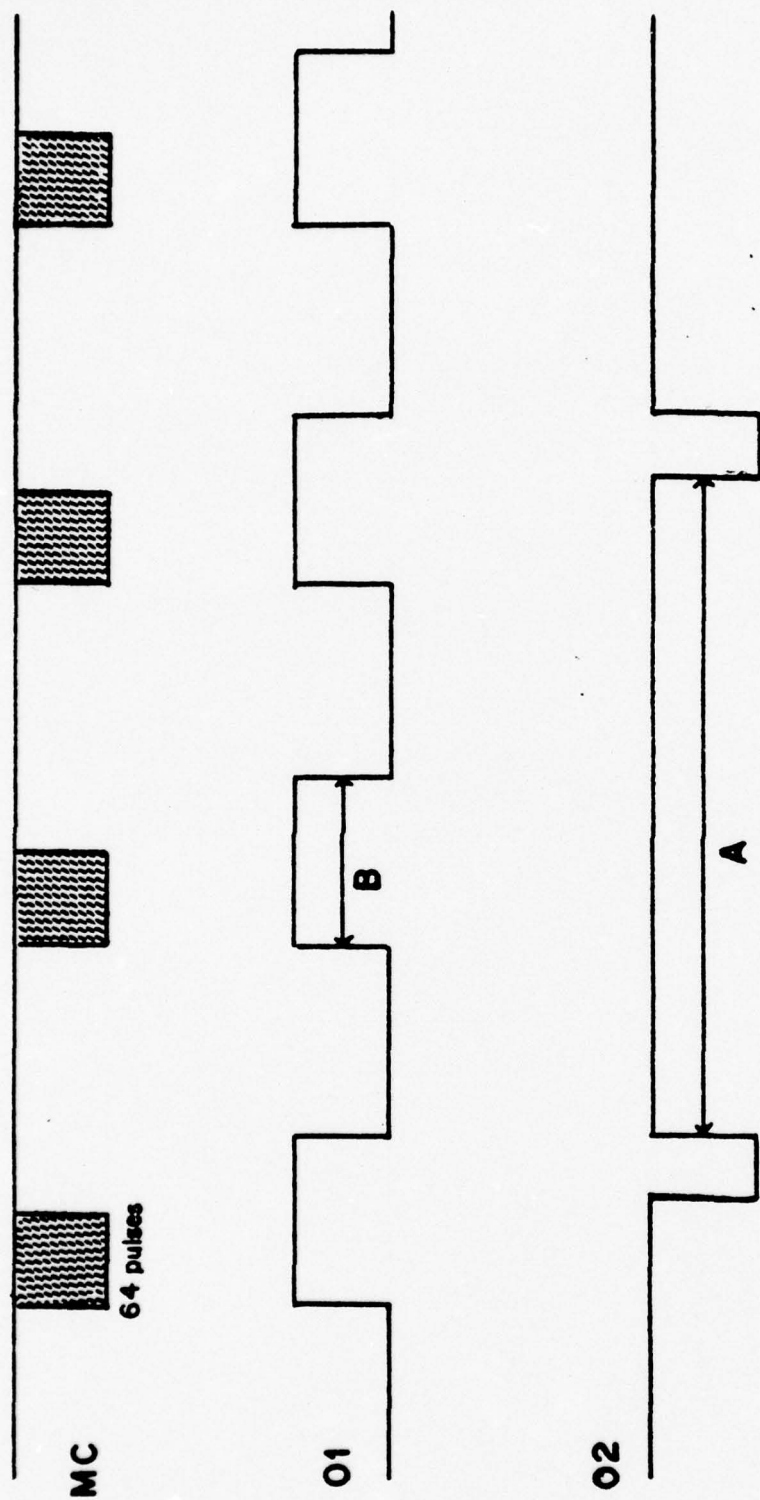
commands to IC-MM. This IC is a quad Tri-State buffer which is used to control the destination of the command clock. The switch opens buffer one which directs the command clock to the ATAC. The CCK7 line closes buffers two and four disabling the command clock input to the KIM-1.

The ATAC supplies the control section with six lines. Five of these are the XAP bits 4, 5, 8, 9, and 13. Using 4, 5, 8, and 9 as address lines to pins 20-23 of IC-DD, a four-to-sixteen demultiplexer, sixteen ( $2^4$ ) unique commands (Table III) were made available. The sixth line, the IOD, and XAP 13 were used as strobes or enables for the demultiplexer. In this way XAP 13 was able to specify this receiver uniquely, and the IOD ensured that addresses and data were stable before passing a command. When both IOD and XAP 13 are low, IC-DD is operational and the output corresponding to the address on pins 20-23 is forced low. At any time that either or both the two strobe lines are high, all outputs of IC-DD are held high and no commands are generated, regardless of the activity on pins 20-23.

At the beginning of the Receiver Control program (Chapter IV), the ATAC sends commands to address the receiver (ADD) and to open the gate for the monitor clock (DST). ADD places a low on pin 2 of IC-E, setting the flip-flop and forcing the ADDA line high. This line activates the receiver's I/O through ICs -JJ, -A, -B, -C, and -LL, as described above. The DST command is passed to

pin 7 of IC-E. This sets this flip-flop and allows the monitor clock (MC) to shift data from the receiver into the storage register during every period two of the receiver's cycle. The MC line is also connected directly to a timing circuit. This circuit produces the pulse described in the early part of this chapter. The first of a pair of monostable multivibrators, IC-Y (Figure 5) is triggered by the first clock pulse of MC. IC-Y outputs a pulse, interval A of timing diagram (Figure 7), which triggers the second. The second's output, interval B, is connected to pin 1 of IC-II, a negative-edge triggered, J-K flip-flop. This IC is wired so that it is set on the output of the second multivibrator and reset by either the the output of the first multivibrator or the command TR. The output of this flip-flop, pin 15, is called the PLP. This line is multiplexed with the least significant bit of the output register and inverted by IC-D for use by the ATAC on line D11.

The RLP pulse is adjustable through variable resistors (trimmers) one and two. Trimmer one controls interval B and trimmer two interval A. In effect, trimmer two varies the position of the pulse and trimmer one its width. The placement and width are the key to proper operation of the interface. The pulse must remain in period three. Although some overlap into period four is allowable it is not desirable, and any overlap into period two could cause



**Figure 7**  
**Interface Timing Diagram**

incorrect operation. At present, the RLP pulse is programmed for every other period three. This allows the receiver to stabilize between samples taken by the computer. If more or less time is desired, the pulse can be set in every, every other, or every third period three by varying trimmer one. Greater time between pulses can be achieved by changing the .47 uF capacitor (hH-7,8) to one of larger value.

When the ATAC is ready to send a word, it loads the input register of the interface using commands DIA, DIB, DIC, DID, and then waits for a high on the D11 line. When RLP is low, D11 is high and the ATAC sends command IRA. This command is routed to a separate monostable multivibrator, IC-Z, by way of multiplexer IC-JJ. The timing circuit provides the trigger pulse in period four which changes the receiver's mode to remote active. It also sets RLP high to prevent any interaction with the ATAC until this cycle of the receiver is complete. During the following period one, the receiver sends the command clock to the input register via ICs -JJ and -MM, and inputs the data word through ICs -JJ and -LL. Meanwhile, the ATAC is waiting for RLP to go low again. When it does, the ATAC closes the MC gate with a DSP command and loads four sixteen-bit words with commands DDA, DDB, DDC, and DDD. Once the receiver word is stored in the ATAC, a DSIA command is sent to open the MC gate. When the operator has finished execution of the Receiver Control program and exits, the ATAC



sends the interface commands ADF and DSP to turn off the address line to the receiver and close the MC gate. The interface is now back in a stand-by status.

In order to set up the interface for operation with the KIM-1, the reset button must be pushed and the computer switch placed in the KIM-1 position. The reset button is unique to KIM-1 interface operation, and is necessary because of the use of the KIM-1's non-maskable interrupt. This interrupt is used to synchronize the KIM-1 with the receiver's command clock. Pressing the reset button places a momentary low on pin 3 of IC-KK, the flip-flop that controls the receiver's address line from the KIM-1. This resets the flip-flop and insures that the command clock output is disabled until required. ICs -JJ and -MM now transfer data from the KIM-1 and not the ATAC. The CCK7 line follows the address line from IC KK and gates the command clock off and on at the proper time. When the KIM-1 is ready to send a word to the receiver, it waits for a low on the RLP line. This line is connected to the maskable interrupt line. This low generates an interrupt and places the KIM-1 in the output program. This routine provides a trigger pulse for the trigger timing circuit and outputs the data synchronously with the command clock. The difference between the ATAC and KIM-1 actions of the interface is due to the position of the switch. The only function the interface serves is to provide reliable and compatible data to the appropriate device, whether it is receiver or

computer.

### 5. INPUT/OUTPUT REGISTERS

These two registers are used for the ATAC only. The registers were designated input or output by their related function with the receiver. They were constructed to provide the necessary, temporary storage while converting parallel and serial data back and forth. Both registers are connected to the PIO bus, with the major difference being the tri-state connections of the serial to parallel, or output register.

The input register (Figure 8) was the easier to implement. It consists of eight 8-bit shift registers with parallel input and serial output. The parallel input comes from the ATAC's PIO bus, which is buffered by schottky inverters to reduce noise. The lines are connected to the ICs in such a way as to load words into two adjacent shift registers simultaneously. This is possible because the shift registers will only latch data in when their respective load line is low. By proper connection of the DIA-DIO lines to pin 1 of the ICs, and coordinating the commands with the data, the output register can be completely and correctly filled. The command clock from the receiver is connected to pin 15 of each of the eight registers. When it is present, it clocks the data through the register exiting through pin 16 of IC-VV. From here, it goes through the control section

at IC-MM and on to the receiver.

The output register (Figure 9) performs the reverse operation. However, in order to separate it into words that are short enough for the ATAC, the data has to be multiplexed before it can be connected to the PIO bus. The Tri-State multiplexers, ICs -I through -L and -U through -X, and the required buffers, ICs -FE through -GG, were used to prevent interaction with the PIO bus when not in use. The timing here is more critical than in the input register system. Before the ATAC begins a read cycle from the output register, the clock signal to the register is stopped (DSP). This prevents the ATAC from reading non-stationary data. All the Tri-State multiplexers are addressed by connecting XAR bits 4 and 5 to pins 2 and 4 respectively. The commands D0A-D0D are ANDed together (NANDed and inverted) and the output connected to all the multiplexers as strobes at pins 1 and 15. When the ATAC reads a word, the XAR bits select the word and the strobe produces it during the microsecond when the PIO bus is available.

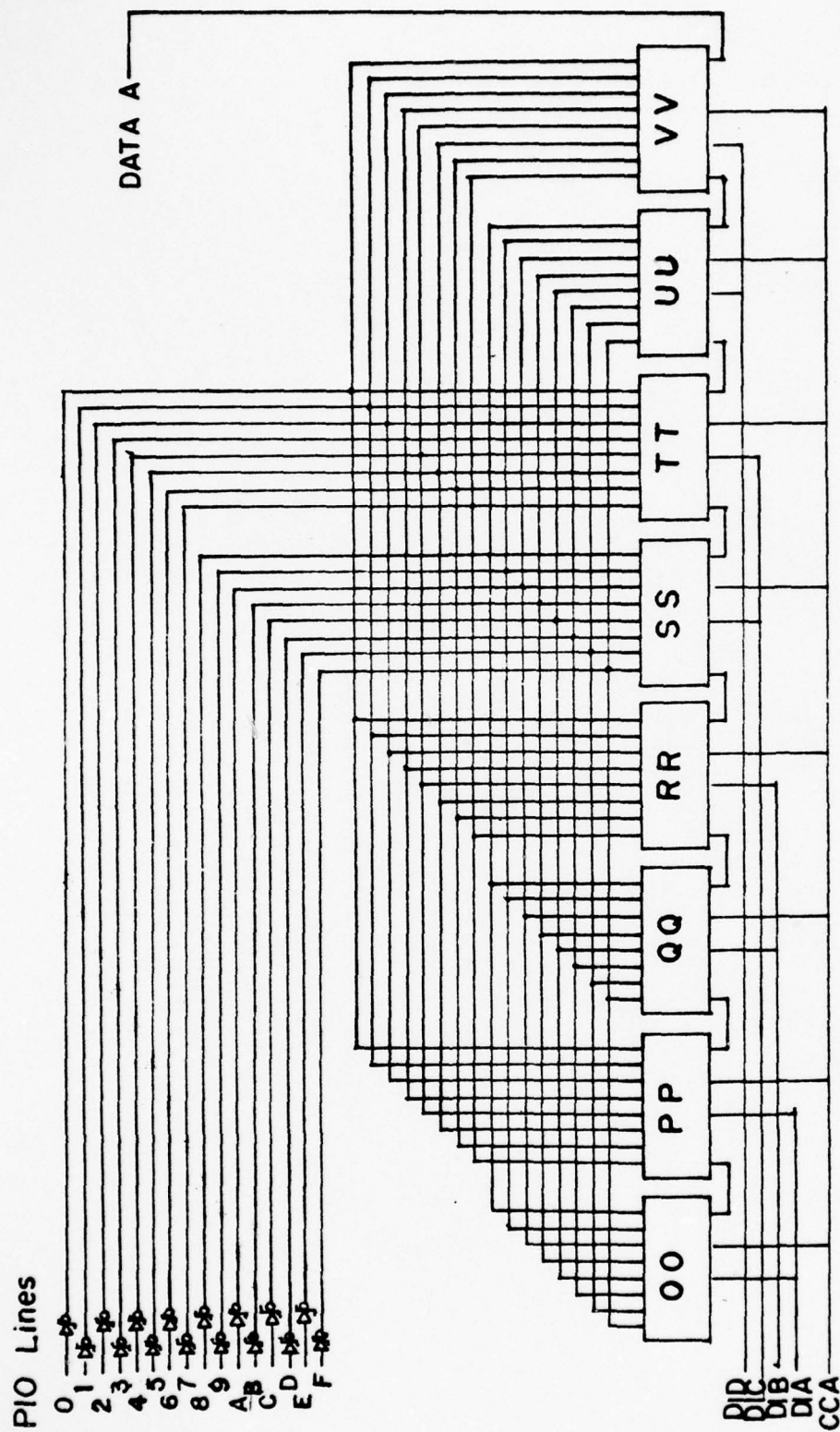


Figure 8  
Input Register



PIO Lines

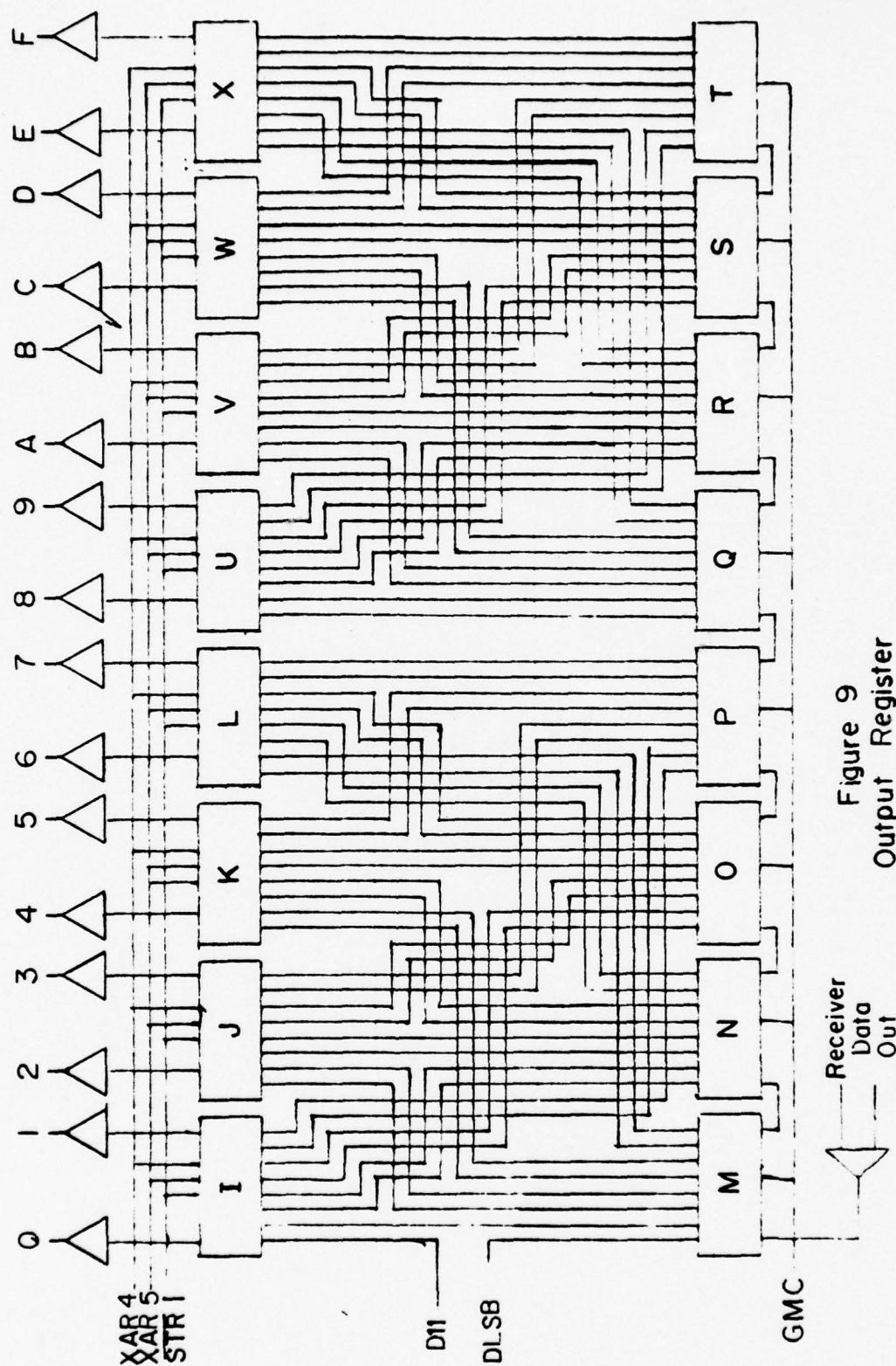


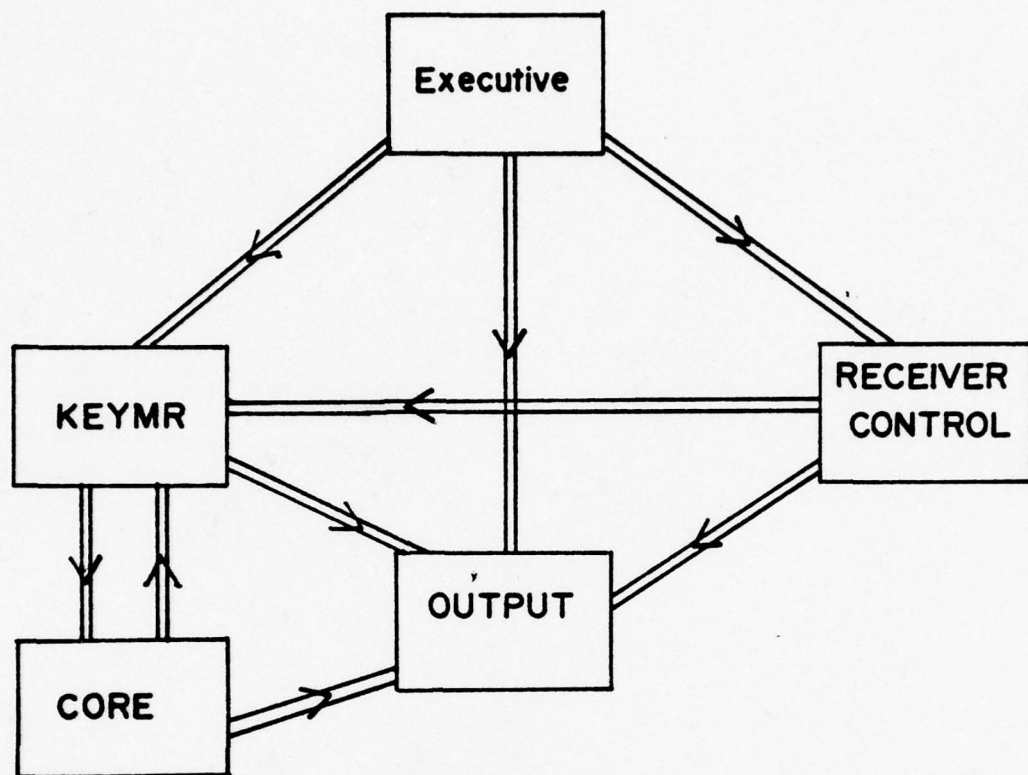
Figure 9  
Output Register

## V. THE PROGRAM

The ATAC program was written in two major sections; a system monitor and a control. The monitor is called the Main System and provides the operator the ability to program the ATAC from the operator's terminal. Receiver Control commands the interface and, therefore the receiver. Both programs were initially written prior to the construction of the interface, so many modifications were made using the Main System and its subroutines. After the interface was built and tested and the Receiver Control section modified to correctly control the tuning of the receiver, the complete program was saved on paper tape (Appendix C). Operation of the computer is discussed in Appendix B and a sample run can be found in Appendix F.

### A. THE MAIN SYSTEM

The Main System section consists of a small executive and a group of interconnected subroutines (Figure 10). The executive provides a basis for the subroutines when the receiver control program is not being executed. It is these subroutines that control the input and output to the operator terminal. The input routine is called KEYMR and the output routine, OUTPUT. OUTPUT converts correctly-formatted computer words into ASCII and displays them on the



⇒ ■ Subroutine Call

Figure 10  
ATAC Program Block Diagram

## I. CORE Commands

- CO -- calls CORE from KEYMR.
- a. DU 'address' -- displays 80 memory locations beginning with 'address'.
  - b. DI 'address' -- displays the contents of memory location 'address'.
  - c. CH 'address' 'value' -- Replaces the contents of memory at 'address' with 'value'.
  - d. CS 'address' -- Beginning at 'address', the contents of memory are replaced with the values typed on the lines following the command. Exit is accomplished by command DO.
  - e. DO -- Returns execution to CORE if in CS, otherwise returns to calling routine.

## II. Receiver Control Commands

- WJ -- Calls Receiver Control from the executive.
- a. 0 -- Set-up - Routine to input values for entry into Receiver.
  - b. 1 -- Displays set-up control word.
  - c. 2 -- Displays last control word sent to receiver.
  - d. 3 -- Displays last control received from receiver.
  - e. 4 -- Sends set-up control word to receiver.
  - f. 5 -- Routine to input scan variables and execute a scan.
  - g. 6 -- Receive and Display control word from the receiver.
  - h. 7 -- Exit program and return to caller.
  - i. 8 -- Reinitialize program as if entering.

Table IV  
AFAC Program Commands



terminal. KEYMR does the reverse, and stores the input in a buffer for use by the caller. KEYMR and OUTPUT were programmed to accept and display only uppercase letters, numerals, and a small number of needed symbols. But, because of the method employed to convert ASCII to machine code, it was found that each lower case letter entered from the keyboard was automatically mapped into its respective upper case twin. This relieves the operator of the responsibility of using the shift key. A part of the KEYMR, called CORE, is available for use by the operator to display and/or change sections of memory. The four available commands in this routine and their functions are displayed in Table IV. Care must be taken not to change memory locations which are used by the Main System. This could result in complete erasure of the ATAC's memory. Without KEYMR, OUTPUT, and CORE, or routines similar to them, it would have been extremely difficult to perform any amount of troubleshooting or modification of the Receiver Control section.

## 8. RECEIVER CONTROL

This section of the system is a branch of the executive. Its main objective is to control both outputs and inputs of the interface from the operator's terminal. To assist those operators with little experience in this system, the Receiver Control section is equipped with uncomplicated

instructions and program safeguards. This produces almost foolproof operation but, it does so at the expense of program simplicity. Discussion of this section is separated into two parts. First a broad description of the complete section is discussed, followed by a detailed look at the two subroutines which interact with the interface.

When the Receiver Control program is entered, it performs five important actions. It initializes all necessary flags; enables the receiver and opens the MC gate; sends and receives a complete receiver word; and displays the instruction set to the operator. After this, it calls on KEYMR and waits for a command. When an input is delivered, the program checks its legality. If it is not a valid command, KEYMR is called again.

A valid command is a numeral between zero and eight (Table IV). These can be separated for discussion into three groups. The display group (0-3) inputs and exchanges information with the operator. The receiver group (4-6) performs operations with the receiver. The final group of commands (7-8) are used to exit or reinitialize the program. Group one has one input and three display commands. Command zero instructs the operator to input the parameters desired. It stores these parameters in memory in the display format, as opposed to control word format. Commands one, two, and three all display parameters. One displays the last parameters set-up by command zero. Two displays the last parameters sent to the receiver. Three displays the last

word received from the receiver. Commands seven and eight make up group three. Seven exits the program entirely and returns to the executive after disabling the receiver. Eight, on the other hand, returns the program to its beginning as if it had just been entered.

The remaining three commands are the most important. Group two commands control the actions of the interface. Command four converts the parameters set-up by command zero into control word format. It then calls the I/O subroutine described below, and outputs and inputs a receiver word. To merely receive a word from the receiver, command six is used. The program calls the input subroutine below and then exits to command three to display the parameters received. Command five scans a band of frequencies selected by the operator in search of a specified signal strength. All other parameters remain the same as those set-up by command zero.

With the exception of the instructions executed when entering and exiting Receiver Control, complete control of the interface and the receiver is resident in approximately forty computer instructions. These forty are grouped into the two subroutines WJR and WJS. WJS sends words to the receiver and WJR receives them. WJS loads the information and addresses to be sent to the receiver into the computer registers. The addresses are then matched to a word of data and sent to the interface input register. The routine now waits for the appropriate signal generated by RLP. When

this is received, a trigger command is sent to load the word into the receiver. At this point the routine checks the value of a counter. This test is to prevent the computer entering an infinite loop if either the interface or receiver is not turned on. If the test is unsatisfactory, the routine prints:

INFINITE LOOP  
PLEASE CHECK RECEIVER AND INTERFACE

and reverts to operator control. If the test is satisfactory, the subroutine automatically continues to WJR. WJR loads another set of addresses into the computer registers. Here, a short wait for the RLP signal is necessary before any action is taken. The MC gate is closed immediately upon receipt of this signal. The receiver word is then loaded into the ATAC by outputting the address on the XAP lines and reading the data on the PIO lines. When the complete word is received, the MC gate is opened. At this point it is necessary to test for command six. This test determines whether the computer is sending and receiving or only receiving. If the execution of both WJS and WJR is being performed, a comparison between the word sent and the word received is necessary. This comparison is skipped if the computer is only executing WJR (command six). The first three control words sent by WJS and received by WJR are used for this comparison, when it is performed. If



any words differ, the computer returns to WJS to repeat the cycle until one of two conditions are met: either the words match or the WJS counter test discussed earlier fails. If the words match, WJP continues on to convert the received control words into the display format and then returns to the caller.

## VI. RECOMMENDATIONS

The system as it stands now is but a beginning. Additions and modifications for future work should include; A/D converters for the receiver outputs; Morse and/or teletype decoders; and an expansion of the computer program. Implementation of either of the first two implies the third. There are some operator assistance program modifications that need to be made. The two that come immediately to mind are (1) a method to abort the scan routine from the operator's console, and (2) the ability to change individual parameters in addition to the set-up command already located in the program. Addition of the A/D converters implies a program increase to decode and process this new data. Switching routines and probably some hardware will be needed for the decoders. The capabilities of the system are limited only by the abilities of the operator and programmer.

## VII. CONCLUSION

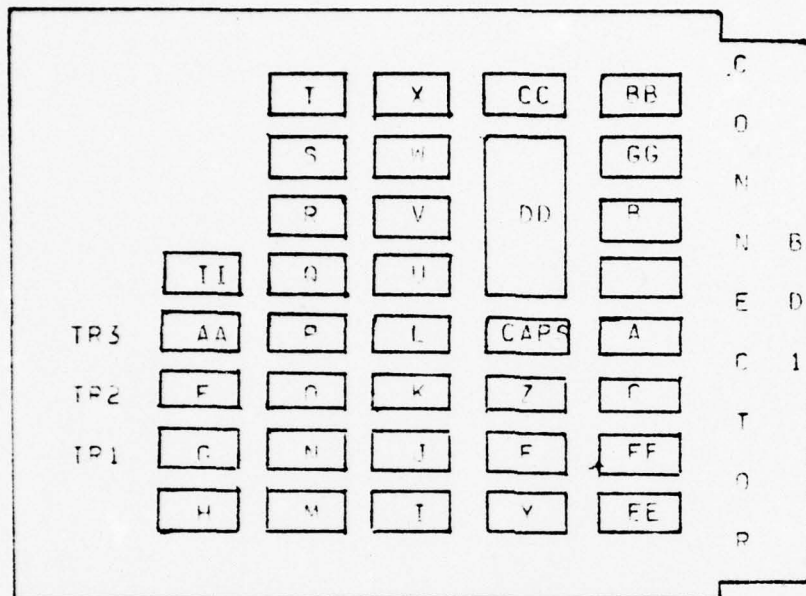
As long as the computer requires only that data obtained from the receiver's word, the interface is flexible enough to provide reliable results. At this time there are no known "bugs" in either the interface or the program. Both have been thoroughly tested to provide the operator with the most dependable system possible.

# APPENDIX A

## INTERFACE WIRING

### A. Board 1

Integrated circuit locations (from Top of board).



### Integrated Circuit

Pin	A	B	C	F	F	G	H
1	8820	8820	8830	7476	7404	7400	74157
1	RD1-M	RD1-K	C-2/Z-3	VCC	M-3	RD2-E	DD-14
2	nc	nc	C-1/C-3	DD-8	H-3	Y-9	II-14
3	BD1-L	BD1-J	C-2/C-4	DD-15	A-6/Y-8	F-11	F-2
4	nc	nc	C-3	VCC	G-5	E-11	I-6
5	nc	nc	BD1-F	VCC	AA-6	F-4	nc
6	F-3/Y-8	M-1	BD1-H	VCC	G-12	F-9	nc
7	GRD	GRD	GRD	DD-7	GRD	GRD	GRD
8	nc	nc	nc	DD-6	I-8	nc	nc
9	nc	nc	nc	VCC	G-6	nc	nc
10	nc	nc	nc	nc	II-3	nc	nc
11	nc	nc	nc	G-4	G-3	F-13	nc
12	nc	nc	nc	VCC	I-15	F-6	nc
13	nc	nc	nc	GRD	G-11	DD-14	GRD
14	VCC	VCC	VCC	nc	VCC	VCC	VCC
15	XXXXXXXX	XXXXXXXX	XXXXXXXX	PD1-Y	XXXXXXXX	XXXXXXXX	XXXXXXXX
16	XXXXXXXX	XXXXXXXX	XXXXXXXX	VCC	XXXXXXXX	XXXXXXXX	XXXXXXXX



# Integrated Circuit

	I	J	K	L	M	N
pin	7214	7214	7214	7214	74164	74164
1	X-15	I-15/J15	J-15/K15	K-15/L15	R-6/M-2	M-13/N-2
2	DD22/J-2	I-2/K-2	J-2/L-2	K-2/U-2	M-1	N-1
3	S-3	S-5	S-10	S-12	F-1	U-6
4	Q-3	Q-5	Q-10	Q-12	I-10	U-10
5	Q-3	Q-5	Q-10	Q-12	J-6	V-6
6	H-4	M-5	M-10	M-12	J-10	V-10
7	EE-1	EE-5	EE-11	FF-1	GRD	GRD
8	GRD	GRD	GRD	GRD	N-8	M-8/O-8
9	EE-3	FE-9	EE-13	FF-3	VCC	VCC
10	M-4	M-6	M-11	M-13	K-6	W-6
11	Q-4	Q-6	Q-11	Q-13	K-10	N-10
12	Q-4	Q-6	Q-11	Q-13	L-6	X-6
13	S-4	S-6	S-11	S-13	L-10	X-10
14	DD23/J14	K-14/I14	J-14/L14	K-14/U14	VCC	VCC
15	F-12/J-1	J-1/K-1	K-1/L-1	L-1/U-1	XXXXXXXXXX	XXXXXXXXXX
16	VCC	VCC	VCC	VCC	XXXXXXXXXX	XXXXXXXXXX

	U	P	Q	R	S	T
pin	74164	74164	74164	74164	74164	74164
1	N-13/O-2	O-13/P-2	P-13/Q-2	Q-13/R-2	R-13/S-2	S-13/T-2
2	O-1	P-1	Q-1	R-1	S-1	T-1
3	T-5	U-5	T-4	U-4	I-3	U-3
4	T-11	U-11	T-12	U-12	T-13	U-13
5	J-5	V-11	J-4	V-4	J-3	V-3
6	J-11	V-11	J-12	V-12	J-13	V-13
7	GRD	GRD	GRD	GRD	GRD	GRD
8	N-8/P-8	Q-8/O-8	P-8/Q-8	Q-8/S-8	R-8/T-8	S-8/F-8
9	VCC	VCC	VCC	VCC	VCC	VCC
10	K-5	W-5	K-4	W-4	K-3	W-3
11	K-11	W-11	K-12	W-12	K-13	W-13
12	L-5	X-5	L-4	X-4	L-3	X-3
13	L-11	X-11	L-12	X-12	L-13	X-13
14	VCC	VCC	VCC	VCC	VCC	VCC

# Integrated Circuit

	U	V	W	X	Y	7
pin	7214	7214	7214	7214	556	555
1	L-15/U15	U-15/V15	V-15/W15	W-15/X15	Y2/Tc-1A	GRD
2	L-2/V-2	U-2/W-2	V-2/X-2	W-2	Y-1/HH-6	PD1-E
3	T-3	T-5	T-10	T-12	HH-5	C-1
4	R-3	R-5	R-10	R-12	VCC	VCC
5	P-3	P-5	P-10	P-12	BD1C/II1	HH-1
6	N-3	N-5	N-10	N-12	Y-9	HH-2/Z-7
7	FF-5	FF-11	GG-1	GG-5	GRD	Z6/Tc-3A
8	GRD	GRD	GRD	GRD	A-6/F-3	VCC
9	FF-9	FF-13	GG-3	GG-9	Y-6	XXXXXXXXXX
10	N-4	N-6	N-11	N-13	VCC	XXXXXXXXXX
11	P-4	P-6	P-11	P-13	HH-4	XXXXXXXXXX
12	R-4	R-6	R-11	R-13	Y-13/HH4	XXXXXXXXXX
13	T-4	T-6	T-11	T-13	Y12/Tc2A	XXXXXXXXXX
14	L-14/V14	U-14/W14	V-14/X14	W-14	VCC	XXXXXXXXXX
15	U-1/V-1	V-1/W-1	W-1/X-1	X-1/Y-1	XXXXXXXXXX	XXXXXXXXXX
16	VCC	VCC	VCC	VCC	XXXXXXXXXX	XXXXXXXXXX

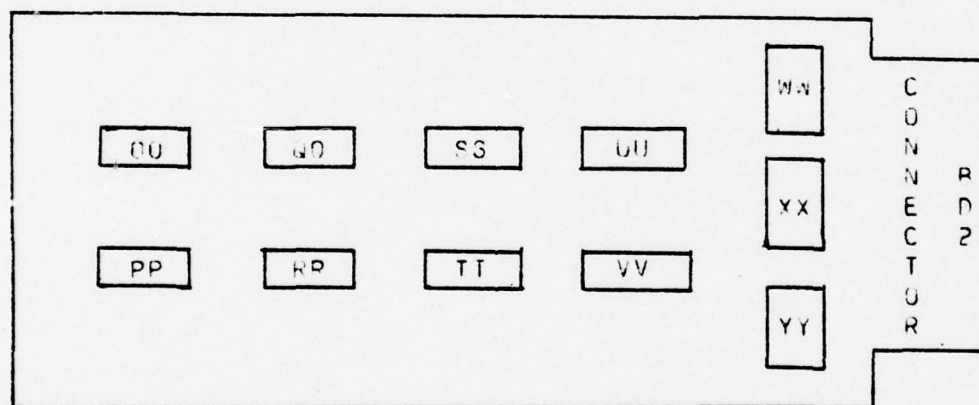
	AA	BB	CC	EE	FF	GG	HH	II
pin	7420	74s04	74s04	7407	7407	7407	CAPS	7476
1	DD-10	CC-6	BD1-17	I-7	L-7	W-7	Z-5	Y-5
2	DD-11	DD-18	DD-23	BD1-1	BD1-7	BD1-13	Z-6	VCC
3	nc	BD1-21	nc	I-9	L-9	W-9	Y-11	F-10
4	DD-9	BB-5	nc	BD1-2	BD1-8	BD1-14	Y-12	VCC
5	DD-13	BB-4	BD1-1	J-7	U-7	X-7	Y-3	nc
6	F-5	DD-19	BB-1	BD1-3	BD1-9	BD1-15	nc	nc
7	GRD	GRD	GRD	GRD	GRD	GRD	Y-2	nc
8	nc	DD-20	nc	BD1-4	BD1-10	BD1-16	GRD	nc
9	nc	BD1-20	nc	J-9	U-9	X-9	GRD	nc
10	nc	DD-21	nc	BD1-5	BD1-11	nc	GRD	nc
11	nc	BD1-19	nc	K-7	V-7	nc	GRD	nc
12	nc	DD-22	nc	BD1-6	BD1-12	nc	GRD	nc
13	nc	BD1-18	nc	K-9	V-9	nc	GRD	GRD
14	VCC	VCC	VCC	VCC	VCC	VCC	GRD	H-2
15	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	nc
16	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	GRD

# Integrated Circuit

		DD 74154	
pin		pin	
1	RD1-P	13	AA-5
2	RD1-X	14	G-13/H-1
3	RD1-W	15	nc
4	RD1-V	16	nc
5	RD1-U	17	F-3
6	E-8	18	BR-2
7	E-7	19	BR-6
8	E-2	20	BR-8
9	AA-4	21	BR-10
10	AA-1	22	BR-12/I-2
11	AA-2	23	CC-2/I-14
12	GRD	24	VCC

## II. Board 2

Integrated Circuit Locations (from Top of board)



# Integrated Circuit

	OO	PP	QQ	RR	SS	TT
pin	74165	74165	74165	74165	74165	74165
1	BD2-A	BD2-A	BD2-B	BD2-B	BD2-C	BD2-C
2	GRD	GRD	GRD	GRD	GRD	GRD
3	WW-2	YY-6	WW-2	YY-6	WW-2	YY-6
4	WW-12	YY-4	WW-12	YY-4	WW-12	YY-4
5	WW-4	YY-2	WW-4	YY-2	WW-4	YY-2
6	WW-10	YY-10	WW-10	YY-10	WW-10	YY-10
7	nc	nc	nc	nc	nc	nc
8	GRD	GRD	GRD	GRD	GRD	GRD
9	PP-10	QQ-10	RR-10	SS-10	TT-10	UU-10
10	VCC	QQ-9	PP-9	QQ-9	RR-9	SS-9
11	XX-2	XX-4	XX-2	XX-4	XX-2	XX-4
12	XX-12	XX-6	XX-12	XX-6	XX-12	XX-6
13	WW-8	XX-8	WW-8	XX-8	WW-8	XX-8
14	WW-6	YY-12	WW-6	YY-12	WW-6	YY-12
15	BD2-21	BD2-21	BD2-21	BD2-21	BD2-21	BD2-21
16	VCC	VCC	VCC	VCC	VCC	VCC

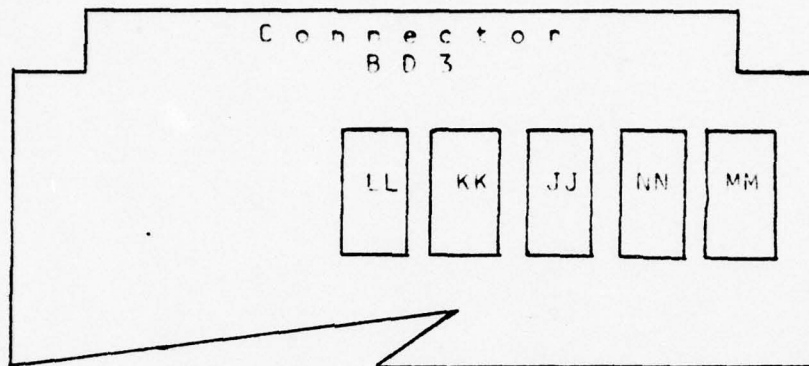
	UU	VV	WA	YX	YY
pin	74165	74165	74s04	74s04	74s04
1	BD2-D	BD2-D	BD2-17	BD2-10	BD2-4
2	GRD	GRD	00-3 *	00-11 *	PP-5 *
3	WW-2	YY-6	BD2-15	BD2-9	BD2-3
4	WW-12	YY-4	00-5 *	PP-11 *	PP-4 *
5	WW-4	YY-2	BD2-13	BD2-8	BD2-2
6	WW-10	YY-10	00-14 *	PP-12 *	PP-3 *
7	nc	nc	GRD	GRD	GRD
8	GRD	GRD	00-13 *	PP-13 *	nc
9	VV-10	BD2-K	BD2-12	BD2-7	nc
10	TT-9	UU-9	00-6 *	nc	PP-6 *
11	XX-2	XX-4	BD3-14	nc	BD2-5
12	XX-12	XX-6	00-4 *	00-12 *	PP-14 *
13	WW-8	XX-8	BD2-16	BD2-11	BD2-6
14	WW-6	YY-12	VCC	VCC	VCC
15	BD2-21	BD2-21	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX
16	VCC	VCC	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX

\* - bus connection - only first connection shown



# C. Board Three

Integrated circuit locations (from Top of board)



## Integrated Circuit

	JJ	KK	LL	MM	NN
pin	74157	7476	8830	74126	8820
1	BD3-1	VCC	LL-2/JJ-7	BD3-1	BD3-5
2	KK-15	BD3-11	LL-1/LL-3	BD3-17	nc
3	BD3-6	BD3-12/20	LL-2/LL-4	BD3-16	BD3-4
4	LL-10	nc	LL-3	JJ-12	nc
5	BD3-8	VCC	BD3-7	GRD	nc
6	BD3-9	nc	BD3-10	BD3-16	MM-9
7	LL-1	nc	GRD	GRD	GRD
8	GRD	nc	BD3-19	BD3-2	nc
9	BD3-13	nc	BD3-18	NN-8	nc
10	BD3-14	nc	LL11/JJ-4	BD3-1	nc
11	nc	nc	LL12/LL10	BD3-3	nc
12	MM13/MM-4	nc	LL13/LL11	MM-9	nc
13	GRD	GRD	LL-12	JJ-12	nc
14	KK-15	nc	VCC	VCC	VCC
15	GRD	JJ-2/JJ14	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX
16	VCC	nc	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX

# D. Connectors

## Circuit Board Edge-connectors

	RD1	RD2	RD3
1	EE-2/RD2-10/CN1-2	GRD	SW1/JJ-1/MM-10
2	EE-4/RD2-11/CN1-3	YY-5/RD1-13	MM-8/RD2-21
3	EE-6/RD2-12/CN1-4	YY-3/RD1-14	MM-11/CN3-1
4	EE-8/RD2-13/CN1-5	YY-1/RD1-15	NN-2/CN2-2
5	EE10/RD2-17/CN1-6	YY-11/RD1-16	NN-1/CN2-3
6	EE12/RD2-16/CN1-7	YY-13/RD1-12	JJ-3/RD1-Y
7	FF-2/RD2-15/CN1-8	XX-9/RD1-11	LL-5/CN2-10
8	FF-4/RD2-14/CN1-9	XX-5/RD1-10	JJ-5/CN3-2
9	FF-6/RD2-9/CN1-10	XX-3/RD1-8	JJ-6/RD2-K
10	FF-8/RD2-8/CN1-11	XX-1/RD1-1	LL-6/CN2-11
11	FF10/RD2-7/CN1-12	XX-13/RD1-2	KK-2/CN3-3
12	FF12/RD2-6/CN1-13	WW-9/RD1-3	KK-3/CN3-4
13	GG-2/RD2-2/CN1-25	WW-5/RD1-4	JJ-9/RD1-F
14	GG-4/RD2-3/CN1-24	WW-11/RD1-8	JJ-10/RD1-P
15	GG-6/RD2-4/CN1-23	WW-3/RD1-7	JJ-11/CN3-5
16	GG-8/RD2-5/CN1-22	WW-13/RD1-6	nc
17	CC-1/CN1-11	WW-1/RD1-5	nc
18	BB-13/CN1-17	nc	LL-9/CN2-12
19	BB-11/CN1-19	nc	LL-8/CN2-11
20	BB-9/CN1-18	nc	KK-3/RESET
21	BB-3/CN1-20	GG-15/RD3-2	nc
22	nc	GRD	VCC
A	GRD	DD-1/RD1-X	GRD
B	nc	GG-1/RD1-W	nc
C	II-14/CN3-6	SS-1/RD1-V	nc
D	nc	UU-1/RD1-U	nc
E	7-2/RD3-13	nc	nc
F	C-5/CN2-9	nc	nc
H	C-6/CN2-8	nc	nc
J	B-3/CN2-7	nc	nc
K	B-1/CN2-6	nc	nc
L	A-3/CN2-5	nc	nc
M	A-1/CN2-4	nc	nc
N	nc	nc	nc
P	DD-1/RD3-14	nc	nc
R	nc	nc	nc
S	nc	nc	nc
T	CC-5/CN1-14	nc	nc
U	DD-5/RD2-D	nc	nc
V	DD-4/RD2-C	nc	nc
W	DD-3/RD2-B	nc	nc
X	DD-2/RD2-A	nc	nc
Y	E-15/RD3-6	nc	nc
Z	VCC	nc	nc

# Cabinet Connectors

pin	CN1	CN2	CN3
1	GRD	GRD	BD3-3 "CCK"
2	BD1-1 "PIO 0"	RD3-4 "CC -"	BD3-8 "DATA K"
3	BD1-2 "PIO 1"	RD3-5 "CC +"	RD3-11 "KAC"
4	BD1-3 "PIO 2"	RD1-M "MC -"	RD3-12 "KAF"
5	BD1-4 "PIO 3"	RD1-L "MC +"	RD3-15 "TRK"
6	BD1-5 "PIO 4"	RD1-K "DO -"	RD1-3 "PLD"
7	BD1-6 "PIO 5"	RD1-J "DO +"	nc
8	BD1-7 "PIO 6"	RD1-H "TR -"	nc
9	BD1-8 "PIO 7"	BD1-F "TR +"	nc
10	BD1-9 "PIO 8"	RD3-7 "DI -"	nc
11	RD1-10 "PIO 9"	RD3-10 "DI +"	nc
12	BD1-11 "PIO 10"	BD3-19 "AD -"	nc
13	BD1-12 "PIO 11"	BD3-18 "AD +"	nc
14	BD1-T "IOU"	nc	GRD
15	nc	nc	nc
16	BD1-17 "XAR 4"	nc	nc
17	BD1-18 "XAR 5"	nc	nc
18	BD1-20 "XAR 9"	nc	nc
19	BD1-19 "XAR 8"	nc	nc
20	BD1-21 "XAR 13"	nc	nc
21	nc	nc	nc
22	BD1-16 "PIO-15"	nc	nc
23	BD1-15 "PIO-14"	nc	nc
24	BD1-14 "PIO-13"	nc	nc
25	BD1-13 "PIO-12"	nc	nc

## E. Discrete Components

### Capacitors

.01 uF	HH-1/HH-14
.2 uF	HH-2/HH-13
.20 uF	HH-3/HH-12
.01 uF	HH-4/HH-11
.01 uF	HH-5/HH-10
.47 uF	HH-7/HH-8

### Resistors

Trimmer			
	1	2	3
A	Y-1	Y-13	Z-7
B	VCC	VCC	VCC
C	VCC	VCC	VCC

APPENDIX B  
ATAC OPERATING INSTRUCTIONS

Power Up

Turn on front panel power then turn on power supplies.

Power Down

'Halt'

'Master Clear'

Power off to supplies, power off to control panel.

Run Program

'Master Clear'

Dial 'IMR'

'AUX REG'

'ENTER' (associated with AUX REG)

'MEMORY'

Set start address +1 in keyboard (Hexadecimal)

'PCP'

'ENTER' (associated with PCP)

'RUN'

Stop a Program

'HALT'

Read Memory (from front panel)

'HALT'

Set desired address in key board

Select 'MAR'

'ENTER' (associated with MAP)

'INC' (increment)

'DEC' (decrement)

Address is displayed above MAR key, data is displayed in red LEDs above MEMORY key.

Use INC or DEC as necessary to arrive at memory location desired.

Write into Memory (from front panel)

'HALT'

Set address desired as described in Read Memory.

Set desired data into keyboard

'ENTER' (associated with MEMORY)

Value in keyboard will be entered into either Memory (MEMORY) or A computer Register (FILE).



Bootstrap Load (paper tape)

'HALT'

'MASTER CLEAR'

'AUX REG'

Dial 'IMR'

'ENTER' (associated with AUX REG)

'MEMORY'

Set '0001 in keyboard

(0001 = Load, 0002 = Verify only)

'RUN'

At end of tape check program status lights (red LEDs  
below PCR and MAR pushbuttons)

0000 = Load good

FFFE = Parity error

FFFD = Verify error

## APPENDIX C

### ATAC PROGRAM ASSEMBLY

Assembly of a program is divided into five parts; writing, producing absolute deck on IBM 360, conversion of absolute deck into ATAC format, punching paper tape, and loading ATAC.

#### A. Writing the program.

Programs for the ATAC must be written in the assembly language described in ATAC manuals Volumes One, and Eight. The finished program must be placed on cards for the IBM 360 in the following format:

LABEL	OPERATION	VARIABLE	COMMENT
BLANKS			

#### B. Producing an absolute deck

The first step is to load the assembler on to the IBM 360 from magnetic tape. This is done by executing program A in Appendix E. This transfers the program from tape to disk and saves it for one year. Once the assembler is stored the

following cards placed in the front of a program written following the instructions in I above will produce an absolute deck and a print-out of the program.

```
//ATACASSM JOB (0729,0194,0052),'CCH ATAC ASSEM,',TIME=1
//ASSEM EXEC PGM=APSS,REGION=220K
//STEPLIB DD DSN=S0729.ATAC.0NF,UNIT=3330,
//          VOL=SER=DISK02,DISP=SHR
//FT06F001 DD SYSOUT=A
//FT07F001 DD SYSOUT=B
//FT05F001 DD DDNAME=SYSIN
//FT08F001 DD UNIT=SYSDA,SPACE=(CYL,1)
//FT09F001 DD UNIT=SYSDA,SPACE=(CYL,(7,2)),
//          DCR=(RECFM=VRS,BLKSIZE=7180,LRECL=92)
//FT10F001 DD UNIT=SYSDA,SPACE=(CYL,(7,2)),
//          DCR=(RECFM=VRS,BLKSIZE=4204,LRECL=42)
//FT20F001 DD UNIT=SYSDA,SPACE=(CYL,(7,2)),
//          DCR=(RECFM=VRS,BLKSIZE=2004,LRECL=500)
//SYSPRINT DD SYSOUT=A
//SYSIN DD *
$JOB
$ASSEM
          IDT  ATAC
```

(place written program here.)

```
          END
$BASE
$LOAD  P
$END
```

The absolute deck is in the form:

```
0500169c0009adbc3109bc9c3109c8bc7109c09c7109d8b60309bbd932/
/e10100009c015a
05101609f49c0109f6ed0008aee1010a02ed000230e10109f7ed0007ae/
/c1070509201258
```

which must be translated for the ATAC. The memory location of the first word is located in the first four columns.

Columns five and six contain the number of word fields on the card. The assembled program is located in columns 7 - 70. The remaining two columns are parity.

#### C. Conversion

The absolute deck received from the IBM 360 is loaded into the PDP-11. After the data from the cards is checked, the conversion program (convert 'filename' 'filename') can be executed. (Program C in Appendix F)

#### D. Punching Paper Tape

This code must then be transferred to the PDP-11 (A) where a paper tape can be punched. Here, the command to punch a tape is:

```
cat 'filename' >/dev/otd
```

#### E. Loading the ATAC

In order to load a tape the RS232 connector must be connected to the Paper Tape reader and the reader set to 1200 baud. The tape is loaded by following the instructions in Appendix B.



# APPENDIX D SAMPLE ATAC OUTPUT

Operator inputs are underlined.

Operator Display	*Comments
EXEC	*Executive echos
+ <u>JDKDKJFJJJnmun</u>	*entries other than
JDKDKJFJJJNMUH	*commands
EXEC	
+ <u>CO</u>	*Entry into CORE
CORE	
+ <u>CH 0F00 0900</u>	*Location 0F00
0F00 0900	*changed to 0900
CORE	
+ <u>DI 0F00</u>	
0F00 0900	
CORE	
+ <u>CS 0F00</u>	*Locations 0F00 to 0F03
+ <u>0256</u>	*changed
+ <u>0123</u>	
+ <u>4567</u>	
+ <u>DO</u>	*completion of change
0F00 0256	
0F01 0123	
0F02 4567	
CORE	
+ <u>DO</u>	*Exit from CORE
+ <u>WJ</u>	*Entry into Receiver
0=SET-UP	*Control
1=DISPLAY TENTATIVE	
2=DISPLAY CONTROL	
3=DISPLAY RECEIVED	
4=ENTER TENTATIVE	
5=SCAN	

6=RECEIVE CONTROL  
7=DONE  
8=REINITIALIZE

RECEIVER CONTROL  
+0

FREQ(HZ)

+1240000  
DETECT MODE  
0=AM  
1=FM  
2=BFO FIXED  
3=BFO VARIABLE  
4=ISB  
5=USB  
6=LSB  
7=AM-ML

+0  
GAIN MODE  
0=HOLD AGC  
2=NORMAL AGC  
3=MANUAL AGC

+0  
IF BANDWIDTH  
1=500 HZ  
2=2 KHZ  
3=4 KHZ  
4=8 KHZ

+4  
RF GAIN  
(PERCENTAGE)

+88

RECEIVER CONTROL

+1  
FREQ = 1240000 HZ  
GAIN MODE = HOLD AGC  
IF BANDWIDTH = 8 KHZ  
DETECT MODE = AM  
BFO FREQ = 455000 HZ  
RF GAIN = 88%

RECEIVER CONTROL  
+2

FREQ = 550000 HZ  
GAIN MODE = NORMAL AGC  
IF BANDWIDTH = 8 KHZ  
DETECT MODE = AM  
BFO FREQUENCY = 455000 HZ  
RF GAIN = 85%

RECEIVER CONTROL

+3

FREQ = 550000 HZ  
GAIN MODE = NORMAL AGC  
IF BANDWIDTH = 8 KHZ  
DETECT MODE = AM  
BFO FREQUENCY = 455000 HZ  
RF GAIN = 85%  
SIGNAL STRENGTH = 66%

RECEIVER CONTROL

+4

RECEIVER CONTROL

+5

SCAN

START FREQ IN HZ

+1000000

END FREQ IN HZ

+1008000

FREQ INCREMENT IN HZ

+1000

SIGNAL STRENGTH %

+67

FREQ = 1001000  
GAIN MODE = HOLD AGC  
IF BANDWIDTH = 8 KHZ  
DETECT MODE = AM  
BFO FREQUENCY = 455000 HZ  
RF GAIN = 88%  
SIGNAL STRENGTH = 72%

RECEIVER CONTROL

+7

EYEC

+

\*Exit from  
\*Receiver Control

# APPENDIX E CONVERSION PROGRAMS FOR THE ASSEMBLER

A. This program is run on the IBM-360 to transfer the ATAC assembler from tape ATI-006 to Disk and stores it there for one year.

```
// (GREEN JOB CARD)
//SYSPRINT DD   SYSOUT=A
//SYSUT1  DD   UNIT=SYSDA,SPACE=(TRK,(40),,CONTIG)
//DA1     DD   UNIT=2314,DSN=S0729.ATAC.ONE,
//          SPACE=(TRK,(50,10,10),,CONTIG),
//          DISP=(NEW,KEEP),VOL=SER=SPOOL3
//T1TAPE DD UNIT=(2400,,DFFER),DISP=(NEW,PASS),
//          LABEL=(3,SL,,IN),
//          DCB=(DCB=2,BLKSIZE=800,LRECL=80,RECFM=FB),
//          VOL=SER=ATI006
//SYSIN    DD   *
COPY      PDS=ATI.APSS.LOADLIB,TO=2314=SPOOL3,
          FROMDD=T1TAPE,FROM=2400=(ATI006,3),
          RENAME=S0729.ATAC.ONE

/*
//BUILD      EXEC PGM=IEHL,REGION=150K,
//          PARM='OVLY,XREF,LET,LIST,SIZE=(256K,20480)'
//SYSPRINT DD   SYSOUT=A
//LIBRARY DD DSN=S0729.ATAC.ONE,UNIT=2314,VOL=SER=SPOOL3,
//          DISP=SHR
//SYSLIB DD DSN=SYS1.FORTLIB,DISP=SHR
//SYSLMOD DD DSN=S0729.ATAC.ONE,
//          UNIT=3330,VOL=SER=DISK02,
//          DISP=(NEW,KEEP),LABEL=RETPD=360,
//          SPACE=(CYL,(5,1,2),RLSE)
//SYSUT1 DD UNIT=SYSDA,SPACE=(TRK,(19,19),,CONTIG),
//          SEP=SYSLMOD
//SYSLIN DD *
INCLUDE LIBRARY(PMIDL)
CHANGE MSIM(IHESAPD)
INCLUDE LIBRARY(APSSMON)
INCLUDE LIBRARY(MSIM4,ASEM5,SIM16A,SIMTR1,SIMIO1,GUL)
INCLUDE LIBRARY(XPLMON)
OVERLAY A1
INSERT MSIMUL,*MSIMOLA,IHENTRY,IHESAP
INSERT MINT,IN,OUT
INSERT IHEDBN,IHEXTD
```



```

INSERT IHERSM,IHECSM
INSERT IHERSK,IHFIOX,IHEIOP,THEIDIO,IHEDOB
INSERT IHEDIR,IHEDCA,IHETOB
INSERT IHEIOA,IHEOCL
INSERT IHERSD,IHEBSF
INSERT IHEJXS
INSERT IHEOSD,IHEOST,IHERST
INSERT IHEVPF,IHEDMA,IHEVER
INSERT IHEDNC,IHEVFD,IHEVFA,IHEVPD,IHEVPB,IHEVSC
INSERT IHEVSD,IHEVFE,IHEDCN,IHEUPB
INSERT IHEVFC,IHEVPE,IHEVPG,IHEVQB,IHEVGC
INSERT IHEABN,IHEIOO,IHEIOF,IHEPRT,IHEVQA,IHESPRT
INSERT IHEREG,IHEERR,IHESI7
INSERT MISEI
OVERLAY A1
INSERT ASSEN,REWIND,REW72,DSKOUT,CARDIN,DISKIN,ERPRT,PRIADD
INSERT WRDATA,PRICOM,PRINOP,WRITEX,REFTIT,PREF,ERTIT
OVERLAY A1
INSERT PARMRD,PRESIM
OVERLAY A1
INSERT SYLTR,NRMTRY,STRTSM,TPAGE
INSERT RDCPD,ABNPMI,ARTHEP,TRACE,HGRAM,HGRAMI,HGRAMS
INSERT IQINIT,ACTIVE,STMTIM
INSERT DEVDTA,ACT,TIME,INT,RAND,DEADT,DEBUG
OVERLAY A2
INSERT LEVEL,DMAIOI,DMAIOA,DMAIOD,RIOIO
INSERT REMACT,DMA,DMAIN,RIO,RIOIM,RIOINT,INTOLY,DMAINT
INSERT DTRAN,PUTACT,RANDOM
OVERLAY A1
INSERT HGPRNT
OVERLAY A1
INSERT LOADER
OVERLAY A1
INSERT LINK,ENTEXT,SLLH
OVERLAY A1
INSERT PLATAC,IOPACK
OVERLAY $OBJECT(REGION)
INSERT OBJECT,INIT,LIB,RCALPH,RCHEX,RCINT
INSERT MDATE
OVERLAY $DUMP(REGION)
INSERT SMDUMP,PAGE
ENTRY MAIN
NAME APSS
/*
//          EXEC PGM=IEBCOPY
//SYSPRINT DD   SYSCUT=A
//SYSUT1  DD   DISP=SHR,UNIT=2314,VOL=SER=SP00L3,
//          DSN=S0729.ATAC.ONE
//SYSUT2 DD   DISP=(NEW,PASS),UNIT=3330,VOL=SER=DISK02,
//          DSN=S0729.ATAC.TWO,

```

```

//          SPACE=(13030,(61,0,14),RLSE),
//          DCB=(RECFM=U,BLKSIZE=13030),
//          LABFL=REIPD=360
//SYSUT3 DD UNIT=SYSDA,SPACE=(TRK,(20,5))
//SYSUT4 DD UNIT=SYSDA,SPACE=(TRK,(20,5))
//SYSIN DD *
COPY OUTDD=SYSUT2,INDD=SYSUT1

```

8. This program converts the IBM-360 absolute deck into correct format for the ATAC.

```

main (argc, *argv)
int argc;
char *argv [1];
(register crctr, index, index);
int stchr;
int tmpary [731];
struct buffr
{int fldes;
int nleft;
char *nexto;
char *buffs [512];
} bufin, bufot, *pnt1, *pnt2;
stchr = 020;
if (argc != 3)
{printf ("Calling arguments are incorrect#");
exit (0);
}
bufin.fldes = open (argv [1], 0);
if (bufin.fldes < 0)
{printf ("Cannot open %s#", argv [1]);
exit (0);
}
pnt1 = &bufin.fldes;
bufot.fldes = creat (argv [2], 0777);
if (bufot.fldes < 0)
{printf ("Cannot open %s#", argv [2]);
exit (0);
}
pnt2 = &bufot.fldes;
putc (stchr, pnt2);
while (crctr >= 0 && index <= 72)
tmpary [index++] = (crctr =getc (pnt1));
index -= 3;
index = 0;
while (index < 4 && index < index)

```

```

       putc (tmpary [index++], pnter2);
index = index + 2;
while (crctr >= 0)
    {while (index < index)
        {if (tmpary [index] == '#')
            index++;
        else
            putc (tmpary [index++], pnter2);
        }
    index = 0;
    while (crctr >= 0 && index <= 72)
        tmpary [index++] = (crctr =getc (pnter1));
    index -= 3;
    index = 0;
}
putc (stchr, pnter2);
fflush (pnter2);
close (bufin.fdcs);
close (bufot.fdcs);
}

```

C. The following program executes the program above and converts the output into the correct code.

```

atrac $1 $2 --
if ! -r $2 exit
mv $2 temp2
tr "[0*]" "[040*]" <temp2 >temp1
tr "[1*]" "[001*]" <temp1 >temp2
tr "[2*]" "[002*]" <temp2 >temp1
tr "[3*]" "[043*]" <temp1 >temp2
tr "[4*]" "[004*]" <temp2 >temp1
tr "[5*]" "[045*]" <temp1 >temp2
tr "[6*]" "[046*]" <temp2 >temp1
tr "[7*]" "[007*]" <temp1 >temp2
tr "[8*]" "[010*]" <temp2 >temp1
tr "[9*]" "[051*]" <temp1 >temp2
tr "[a*]" "[052*]" <temp2 >temp1
tr "[b*]" "[013*]" <temp1 >temp2
tr "[c*]" "[054*]" <temp2 >temp1
tr "[d*]" "[015*]" <temp1 >temp2
tr "[e*]" "[016*]" <temp2 >temp1
tr "[f*]" "[057*]" <temp1 >$2
rm temp1 temp2

```

APPENDIX F  
ATAC PROGRAM

The following programs are listings of the Main System and Receiver Control programs for the ATAC. The assembly language is to the right of the absolute listing of the first three columns.





ATAC	LOC	OBJECT CODE	CARD IMAGE	TIME: 15:22:49	03/21/77	PAGE	CARDNUM
				COMBINE FIRST TWO BYTES OF COMMAND			55
	0117	A446	IOR R,EU,EL	SEE IF REQUEST FOR WJ			56
	0118	B106 776A	CMP I,EU,0776A	GO CALL WJ			57
	011A	C102 012A	BRCL EQ,P12				58
	011C	0000	NOP	PATCH AREA FOR ANOTHER REQUEST			59
	011D	0000	NOP				60
	011E	0000	NOP				61
	011F	0000	NOP				62
							63
							64
							65
							66
							67
	0120	BCF0 0136	LDRM D,0,EXECS,16	RESTORE REGISTERS			68
	0122	ED00 0230	BAL I,0,OUTPUT	ECHO INPUT BUFFER			69
	0124	E101 014A	LDR I,1,EXCRLP	GET ADDRESS OF CR/LP BUFFER			70
	0126	ED00 0230	BAL I,0,OUTPUT	OUTPUT CR/LP			71
	0128	C107 0100	BRC I,7,EXEC	GO TRY AGAIN			72
							73
							74
	012A	ED00 0500	BAL I,RET,WJ	GO TO WJ			75
	012C	C107 0100	BRCL U,EXEC				76
							77
							78
							79
							80
							81
							82
							83
							84
							85
							86
							87
							88
							89
							90
							91
							92
							93
							94
							95
	0136		EXECS DS 20	SAVE AREA FOR REGISTERS			96
	014A	0001	EXCRLF DC 1	CR/LF			97
	014B	000A	DC 0				98
	014C	0000	DC 0				99
	014D	0003	DC 3	COUNT			100
	014E	4558	DC 04558	EX			101
	014F	4543	DC 04543	EC			102
	0150	0000	DC 0	NULL			103
							104
							105
							106
							107

LOC OBJECT CODE

CARD IMAGE

PAGE

CARDNUM

```
*****
* SYSTEM EQUATES
*
* THESE ARE EQUATES THAT ARE USED FOR LINKAGE BETWEEN
* PROGRAMS OR THAT ARE USED BY AT LEAST TWO PROGRAMS IN
* THE SYSTEM
*
*****
RET EQU 0 RETURN REGISTER
*****
*****
* KEYMR
*
* ROUTINE TO READ DATA FROM THE KEYBOARD
*
* CALLING PROCEDURE:
* BAL I,0,KEYMR
*
* INPUTS:
* NONE
*
* OUTPUTS:
* REG 1
*
* ADDRESS OF BUFFER CONTAINING THE KEYBOARD
* ENTRY, ONE CHARACTER PER WORD, RIGHT
* JUSTIFIED, ASCII
* THE FIRST WORD OF THE BUFFER CONTAINS THE
* NUMBER OF CHARACTERS IN THE KEYBOARD
* ENTRY BUFFER
*
* ROUTINES CALLED:
* OUTPUT
*
* THIS ROUTINE PRESERVES NO REGISTERS
*
*****
*****
* ESTABLISH EQUATES
*
*****
KRET EQU 0
KBUF EQU 1
KPC EQU 5
KPH EQU 6
KOR EQU 7
KIR EQU 8
KOUT EQU 9
KIN EQU 10
KVI EQU 11

RETURN REGISTER
ADDRESS OF BUFFER HOLDING KEYBOARD
ENTRY
POSITION COUNTER FOR NEXT INPUT
INPUT FROM KEYBOARD (CURSOR)
MAX POSITION USED IN KEYBOARD ENTRY
(NUMBER OF CHARACTERS ENTERED)
OUTPUT REGISTER
INPUT REGISTER
OUTPUT DEVICE ADDRESS
INPUT DEVICE ADDRESS
VARIABLE 1
```

70



03/21/77

TIME: 15:22:49

ATAC

LOC

CARD IMAGE

OBJECT CODE

LOC

0179	A10E 007F	.	AND	I, KDATA, 0007F	214
017B	208E	.	CMP	IS, KDATA, 008	215
017C	C105 0184	.	BRCL	NE, KMR6	216
017E	6105 0169	.	ADD	IS, KPC - 1	217
017F	C105 0169	.	BRCL	WZ, KMR3 - 1	218
0181	4015	.	LDR	IS, KPC, 1	219
0182	C107 0169	.	BRCL	U, KMR3	220
0184	21CE	KMR6	CMP	IS, KDATA, 01C	221
0185	C105 0190	.	BRCL	NE, KMR8	222
0187	6015	KMR7	ADD	IS, KPC 1	223
0188	B105 0050	.	CMP	I, KPC 80	224
018A	C106 0169	.	BRCL	LE, KMR3	225
018C	E105 0050	.	LDR	I, KPC 80	226
018E	C107 01B9	.	BRCL	U, KMR11	227
0190	20DE	KMR8	CMP	IS, KDATA, 00D	228
0191	C102 01B9	.	BRCL	EQ, KMR11	229
0193	22EE	.	CMP	IS, KDATA, 02E	230
0194	C102 01B1	.	BRCL	EQ, KMR10	231
0196	220E	.	CMP	IS, KDATA, 020	232
0197	C102 01B1	.	BRCL	EQ, KMR10	233
0199	230E	.	CMP	IS, KDATA, 030	234
019A	C104 01AB	.	BRCL	LT, KMR9	235
019C	239E	.	CMP	IS, KDATA, 039	236
019D	C106 01B1	.	BRCL	LE, KMR10	237
019F	241E	.	CMP	IS, KDATA, 041	238
01A0	C104 01AB	.	BRCL	LT, KMR9	239
01A2	25AE	.	CMP	IS, KDATA, 05A	240
01A3	C106 01B1	.	BRCL	LE, KMR10	241
01A5	261E	.	CMP	IS, KDATA, 061	242
01A6	C104 01AB	.	BRCL	LT, KMR9	243
01A8	27AE	.	CMP	IS, KDATA, 07A	244
01A9	C106 01B1	.	BRCL	LE, KMR10	245
01AB	E101 022C	.	LDR	I, KMR9	246
01AD	E000 0230	.	BRCL	I, KMR9	247
01AF	C107 0153	.	BRCL	U, KMR11	248
*****					249
: ILLEGAL ENTRY					250
: *****					251
: *****					252
: *****					253
: *****					254
: *****					255
: *****					256
: *****					257
: *****					258
: *****					259
: *****					260
: *****					261
: *****					262
: *****					263
: *****					264
: *****					265
: *****					266

PAGE  
CARDNUM

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CARD IMAGE

ATAC  
LOC OBJECT CODE

```

*****
: VALID ENTRY - PUT IN BUFFER
: *****
KMR10 9B5E 01D7 STR DX,KDATA,KBUFFER,KPC PUT DATA IN BUFFER
      B056 01B7 CMP R,KPM,KPC COMPARE MAX USED WITH LAST POSITIO
      E056 01B6 LDR R,KMR7 GO INCREMENT POSITION COUNTER
      C107 01B7 BRCL U,KMR7 PM = PC
      KEEP GETTING DATA
:
: *****
: EXIT
: *****
KMR11 9C06 01D7 STR D,KPM,KBUFFER PUT COUNT IN BUFFER
:
: THIS IS THE SEQUENCE FOR CALLING 'CORE' (UTILITY TO DISPLAY AND
: CHANGE CORE IN ORDER TO CALL TO THAT PROGRAM IS NO LONGER DESIRED.
: REMOVED WHEN A CALL TO THAT PROGRAM IS NO LONGER DESIRED.
KMR30
      E01B 4005 LDR R,KPC,0
      4005 01B8 ADD R,KV1,KV1,KPC
      501B 01B8 LDR R,KV2,KV1,KPC
      6FF6 01D3 BRCL U,KMR7
      C106 01B0 CMP R,KMR7,0
      C102 01B0 ADD R,KV2,KV2,0
      601B 01B0 BRCL U,KMR7
      ADD R,KV1,KV1,1
      LDR R,KV3,KV1,KPC
      SHS LL,KV3,8
      SHS LL,KV3,8
      SHS RL,KV3,8
      ADD R,KV2,KV2,0
      CMP R,KV2,0636F
      BRCL U,KMR7
      LDR R,KMR7
      BRC I,7,CORE
KMR12 01D3 01D6 LDR D,KRET,RETURN
      BF07 01D5 BRC R,7,KRET
:
: *****
: DATA
: *****
RETURN DS 1
: *****
:
: RETURN ADDRESS STORAGE

```

ATAC	LOC	OBJECT CODE	CARD IMAGE	TIME: 15:22:49	03/21/77	PAGE	CARDNUM
			KEYBOARD ENTRY BUFFER				320
			*****				321
			KBUFFER DC 80				322
			DS 80				323
	01D7	0050					324
	01D8						325
			*****				326
			START SYMBOL BUFFER				327
			*****				328
			KBSTRT DC 3				329
			DC 0000A				330
	0228	0003	DC 002B				331
	0229	000A	DC 00000				332
	022A	002B	DC 00000				333
	022B	0000	*****				334
			ILLEGAL CHARACTER BUFFER				335
			*****				336
			KBILL DC 3				337
			DC 00A07				338
	022C	0003	DC 00707				339
	022D	0A07	DC 00000				340
	022E	0707	*****				341
	022F	0000	*****				342
			*****				343
			ROUTINE TO OUTPUT TO THE TTY/CRT				344
			*****				345
			CALLING PROCEDURE:				346
			BAL I,0,OUTPUT				347
			*****				348
			INPUTS:				349
			REG 1 ADDRESS OF BUFFER TO BE OUTPUT				350
			*****				351
			THE BUFFER MUST BE SET UP IN THE FOLLOWING MANNER:				352
			WORD 1 N = NUMBER OF WORDS IN BUFFER TO BE OUTPUT				353
			WORDS 2-N ASCII DATA TO BE OUTPUT, TWO ASCII				354
			CHARACTERS PER WORD				355
			*****				356
			OUTPUTS:				357
			NONE				358
			ROUTINES CALLED:				359
			NONE				360
			*****				361
			THIS ROUTINE PRESERVES NO REGISTERS				362
			*****				363
			*****				364
			*****				365
			*****				366
			*****				367
			*****				368
			*****				369
			*****				370
			*****				371
			*****				372

PAGE	CARDNUM
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
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90	90
91	91
92	92
93	93
94	94
95	95
96	96
97	97
98	98
99	99
100	100

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**CARD IMAGE**

ATAC	LOC	OBJECT CODE
------	-----	-------------

\*\*\*  
ESTABLISH EQUATES  
\*\*\*

	EQU	1
	EQU	5
	EQU	6
	EQU	7
	EQU	8
	EQU	9
	EQU	10
	EQU	11
	EQU	12
	EQU	13
	EQU	14
	EQU	15

ADDRESS OF BUFFER TO OUTPUT  
 OUTPUT BUFFER ADDRESS  
 INPUT BUFFER ADDRESS  
 OUTPUT DEVICE ADDRESS  
 INPUT DEVICE ADDRESS  
 INPUT BUFFER LOWER BYTE  
 INPUT BUFFER UPPER BYTE  
 NUMBER OF WORDS TO OUTPUT  
 NUMBER OF WORDS TO INPUT  
 UPPER BYTE INDEX  
 LOWER BYTE INDEX  
 STATUS  
 WORD TO OUTPUT TO TTY

```

**      **      **      **      **      **      **      **      **      **
INITIALIZE AND SET UP CONSTANTS
**      **      **      **      **      **      **      **      **      **

```

[illegible]

```

INDEX FOR STORING UPPER BYTE
HHINDEX FOR STORING LOWER BYTE
HINDEX INPUT DEVICE ADDRESS
HOUTINDEX OUTPUT DEVICE ADDRESS
GET INPUT WORD COUNT
INITIALIZE COUNT
COMPARE WORD COUNT WITH ZERO
GET OUT IF COUNT LESS THAN ZERO
COMPARE WITH MAX VALUE
IF IN LIMIT KEEP GOING
SAVE ORIGINAL COUNT
ONLY OUTPUT 40 WORDS
IN OUTPUT WORD COUNT
DOUBLE FOR OUTPUT WORD COUNT
GET OUTPUT BUFFER ADDRESS

```

```
**      **      **      **      **      **      **      **      **
```

TRANSFER INPUT BYTE BUFFER TO OUTPUT WORD BUFFER

```
**      **      **      **      **      **      **      **      **
```

0246	6011	OUT1	ADD	IS,RUFAD,1
0247	51C9		LDR	RX,VU,VU,6
0248	E098		LDR	RX,VU,VU,6
0249	AE78		SHS	LL,V1,8
024A	AD78		SHS	RL,V1,8
024B	AD79		SHS	RL,VU,8
024C	15C9		STR	RX,VU,VU,BO
024D	15D8		STR	RX,V1,V1,BO

```

INCREMENT INPUT POINTER TO NEXT ENTRY
GET INPUT WORD IN UPPER BYTE REGISTER
CLEAR INPUT LOWER BYTE REGISTER ALSO
RIGHT JUSTIFY UPPER BYTE
RIGHT JUSTIFY LOWER BYTE
STORE UPPER BYTE AS FULL WORD
STORE LOWER BYTE AS FULL WORD

```



ATAC	LOC	OBJECT CODE	CARD IMAGE	TIME: 15:22:49	03/21/77	PAGE	CARDNUM
024E	6075		ADD IS,BO,2				426
024F	6FEB		ADD IS,WI,-1				427
0250	C101 0246		BRCL GT,OUT1				428
			*****				429
			OUTPUT WORD BUFFER				430
			*****				431
			*****				432
			*****				433
			*****				434
0252	E105 026B		LDR I,BO,BUPOUT				435
0254	8C6E		RIN STAT,WIN				436
0255	9E0E 1000		IF,STAT,01000				437
0257	C105 0254		BRCL NE,OUT2				438
0259	B75F 0000		LLC DX,WOUT,0,BO				439
025B	A10F 01FF		AND I,WOUT,0,BO				440
025D	D97F		ROUT WOUT,VOUT				441
025E	6015		ADD IS,BO,1				442
025F	6F8A 0254		ADD IS,W0,-1				443
0260	C101		BRCL GT,OUT2				444
			*****				445
			EXIT				446
			*****				447
			*****				448
0262	F20B 026A		LDR D,WI,COUNT				449
0264	C102 0269		BRCL Z,OUT4				450
0266	6D8B		ADD IS,WI,-40				451
0267	C107 0237		BRCL U,OUT5				452
0269	BF07		BRC R,7,RET				453
			*****				454
			*****				455
			*****				456
			*****				457
			*****				458
026A		COUNT DS 1	SAVE LOCATION FOR EXCESS COUNT				459
026B		BUFOUT DS 80	OUTPUT BUFFER				460
			*****				461
			*****				462
			*****				463
			*****				464
			*****				465
			*****				466
			*****				467
			*****				468
			*****				469
			*****				470
			*****				471
			*****				472
			*****				473
			*****				474
			*****				475
			*****				476
			*****				477
			*****				478



ATAC	LOC	OBJECT CODE	CARD IMAGE	GET RETURN ADDRESS	CARDNUM
02DB	E200	02E1	LDR D,RET,HEXRTN	RETURN	532
02DA	BF07		BRC R,7,RET		533
			*****		534
			.. CONVERT ONE DIGIT		535
			*****		536
02DB	20A4	02DF	HEXA1 CMP IS,V1,00A	COMPARE WITH HEX 'A'	537
02DC	C104		BRC L,HEXA2	BRANCH IF LESS	538
02DE	6074		ADD IS,V1,7	ADD 7 TO VALUE	539
02DF	6304		ADD IS,V1,030	ADD HEX '30'	540
02F0	BF07		BRC R,7,RET	GO BACK TO WHERE CALLED FROM	541
			****		542
			.. DATA		543
			.. ****		544
02E1			HEXRTN DS 1	SAVE LOCATION FOR RETURN ADDRESS	545
			*****		546
			.. AHX		547
			*****		548
			.. ROUTINE TO CONVERT FOUR (4) OR LESS DIGITS IN ASCII		549
			.. CODE TO A TRUE HEX VALUE FOR THE MACHINE. SIGN OF THE		550
			.. VALUE MUST BE HANDLED BY THE CALLING ROUTINE.		551
			.. CALLING PROCEDURE:		552
			.. BAL I,0,AHAX		553
			.. INPUTS:		554
			.. REG 1 ADDRESS OF FIRST CONSECUTIVE LOCATION IN		555
			.. CORE WHERE THE ASCII CHARACTERS ARE LOCATED		556
			.. (ONE CHARACTER PER CORE LOCATION)		557
			.. OUTPUT:		558
			.. REG 2 HEX VALUE		559
			.. ROUTINES CALLED:		560
			.. NONE		561
			.. REGISTERS 8 THROUGH 16 ARE PRESERVED		562
			.. *****		563
			.. ESTABLISH EQUATES		564
			.. *****		565
			.. AHADD EQU 1	ADDRESS OF ASCII CHARACTERS	566
			.. AHOUT EQU 2	OUTPUT HEX VALUE	567
			.. AHV1 EQU 5	VARIABLE 1	568
			.. *****		569
			.. *****		570
			.. *****		571
			.. *****		572
			.. *****		573
			.. *****		574
			.. *****		575
			.. *****		576
			.. *****		577
			.. *****		578
			.. *****		579
			.. *****		580
			.. *****		581
			.. *****		582
			.. *****		583
			.. *****		584

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LOC	OBJECT CODE	CARD IMAGE	VARIABLE 2	CARDNUM
02E2		AHV2		585
02E3		AHV2		586
02E4		AHV2		587
02E5		AHV2		588
02E6		AHV2		589
02E7		AHV2		590
02E8		AHV2		591
02E9		AHV2		592
02EA		AHV2		593
02EB		AHV2		594
02EC		AHV2		595
02ED		AHV2		596
02EE		AHV2		597
02EF		AHV2		598
02F0		AHV2		599
02F1		AHV2		600
02F2		AHV2		601
02F3		AHV2		602
02F4		AHV2		603
02F5		AHV2		604
02F6		AHV2		605
02F7		AHV2		606
02F8		AHV2		607
02F9		AHV2		608
02FA		AHV2		609
02FB		AHV2		610
02FC		AHV2		611
02FD		AHV2		612
02FE		AHV2		613
02FF		AHV2		614
0300		AHV2		615
0301		AHV2		616
0302		AHV2		617
0303		AHV2		618
0304		AHV2		619
0305		AHV2		620
0306		AHV2		621
0307		AHV2		622
0308		AHV2		623
0309		AHV2		624
030A		AHV2		625
030B		AHV2		626
030C		AHV2		627
030D		AHV2		628
030E		AHV2		629
030F		AHV2		630
0310		AHV2		631
0311		AHV2		632
0312		AHV2		633
0313		AHV2		634
0314		AHV2		635
0315		AHV2		636
0316		AHV2		637

CLEAR REGISTER  
 SET UP COUNTER  
 SET UP ZERO REGISTER  
 GET ASCII CHARACTER  
 COMPARE WITH SPACE  
 DON'T TRANSLATE SPACES  
 MOVE DIGIT OVER  
 COMPARE WITH MIN LETTER  
 SKIP IF NUMERIC  
 INCREMENT ALPHA  
 CLEAR ALL BUT DIGIT  
 PUT IN OUTPUT REGISTER  
 DECREMENT COUNTER  
 DONE  
 INCREMENT CHARACTER ADDRESS  
 KEEP GOING  
 GET OUT

\*\*\*\*\*  
 \*\*\* WARNING \*\*\*\*\*  
 THIS ROUTINE SHOULD ONLY BE CALLED BY 'KEYMR'. THERE ARE  
 SPECIAL CONSIDERATIONS IN CALLING WHICH ARE TAKEN INTO  
 ACCOUNT BY 'KEYMR'. (TAKE SPECIAL NOTE OF REGISTER 2 WHEN  
 'CORE' IS CALLED AND THE WAY 'CORE' EXITS THROUGH 'KEYMR'.  
 MAY BE INITIATED BY THE OPERATOR AT ANY TIME WHEN THE  
 KEYBOARD IS ACCEPTING DATA BY TYPING 'CORE'.  
 ENTERED. IT REMAINS IN CONTROL UNTIL RELEASED BY THE  
 TYPED COMMAND 'DONE'. THE COMMANDS AND FUNCTIONS ARE  
 AS LISTED:  
 COMMAND FUNCTION  
 DONE 'ADD' PRINTS 10 LINES OF 8 VALUES  
 \*\*\*\*\*



```

*
* OP CORE STARTING WITH THE
* ADDRESS SPECIFIED 'ADD'
* MUST BE HEXIDEcimal - ALPHA
* CHARACTERS IN UPPER CASE.
* 'DUMP' MUST BE TYPED IN LOWER
* CASE LETTERS
*
* CHANGES THE CONTENTS OF THE
* CORE LOCATION WHOSE ADDRESS
* IS SPECIFIED TO THE VALUE
* SPECIFIED
*
* DISPLAYS THE CONTENTS OF THE
* CORE LOCATION IN 'ADD'
*
* CS 'ADD'
*
* CALLING PROCEDURE:
* BAL 1,0,CORE
*
* INPUTS:
* NONE
*
* OUTPUTS:
* NONE
*
* ROUTINES CALLED:
* KEYMR
* OUTPUT
* HEXA
* AHX
*
* THIS ROUTINE PRESERVES NO REGISTERS
*
* *****
* ESTABLISH EQUATES
* *****
*
* CADD EQU 1
* CHV EQU 1
* CA1 EQU 2
* CA2 EQU 3
*
* ADDRESS OF BUFFER RETURNED
* HEX VALUE TO INPUT TO HEXA
* ASCII MSD RETURNED BY HEXA
* ASCII LSD RETURNED BY HEXA

```

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**PAGE**

**CARDNUM**

ATAC

LOC

**OBJECT CODE**

**CARD IMAGE**

VARIABLE 3  
MAX NO. CHARACTERS INPUT BY KFYMR  
PATH FLAG  
BLANK FLAG  
FIELD2  
CONSTANT 0 FOR SPACE  
ASCII CODE  
VARIABLE 1  
VARIABLE 2  
COMMAND  
FIELD 1

```
SAVE REGISTER 2      •
GET A ZERO          SEQUENTIAL CHANGE FLAG
INITIALIZE          ADDRESS FOR TITLE
GET BUFFER           COMMAND
OUTPUT TITLE        CONSTANT
SET UP SPACE CODE   FIELD 1
SET UP ZERO         FIELD 2
ZERO COMMAND REGISTER
ZERO FIELD 1
ZERO FIELD 2
ZERO PATH FLAG
```

```

GET NO. OF ENTRIES IN BUFFER
SET FLAG FOR READY
INCREMENT BUFFER ADDRESS
DECREMENT CHARACTER COUNTER
DONE
GET A CHARACTER FROM THE BUFFER
COMPARE WITH SPACE
KEEP GOING IF SPACE
SEEK IF IN MIDDLE OF ENTRY
IN ENTRY, KEEP LOOKING
GET PROCESSING ADDRESS
PROCESS ACCORDING TO FIELD FOUND

```

CV3	EQU	5
CMAX	EQU	6
CINDX	EQU	7
CFLG	EQU	8
CF2	EQU	9
CZERO	EQU	10
CSPACE	EQU	11
CV1	EQU	12
CV2	EQU	13
CMD	EQU	14
CF1	EQU	15

```

CORE
C1
STR LDR D,2,CSAVE
STR LDR D,CV1,0
STR LDR D,CV1,CSPG
LDR LDR I,CADD,CITL
LDR LDR I,RET,OUTL
BAL BAL I,RET,KEYR
LDR LDR I,C2,ACE,02020
LDR LDR I,C2,ZERO,0
LDR LDR I,C2,0,0
LDR LDR I,C2,1,0
LDR LDR I,C2,2,0
LDR LDR I,C2,6,0
LDR LDR I,C2,7,0
LDR LDR I,C2,ND,0

```

```
*****  
**TRANSLATE COMMAND**  
*****
```

```

LDR      RA, CHAX, CZERO, CADD
LDR      IS, CFLAG, 0
LDR      IS, CADD, 1
ADD      IS, CHAX, -1
BRCL     MP, C6A
LDR      RP, C6A, CZERO, CADD
LDR      IS, CV1, 020
CMP      EQ, C2
CMP      EQ, CFLAG, 0
BRCL     NZ, C3

LDR      DX, RET, CFLAG, CINDEX
BR      B, RET

```

BRANCH TABLE

02F8	9C02	03D3
02FA	400C	0412
02FB	9C0C	0405
02FC	E101	0230
02FD	ED00	0151
02FE	ED00	2020
0301	E10B	
0303	400A	
0305	400E	
0306	400F	
0307	400F	
0308	4009	
0309	4008	
030A	4007	

030B	51A6	
030C	4008	
030D	6011	0327
030E	6PF6	
030F	C106	
0311	51AC	
0312	220C	030C
0313	C102	
0315	2008	030D
0316	C105	
0318	E370	031B
031A	BP07	

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ATAC	LOC	OBJECT CODE	CARD IMAGE	COMMAND FIELD	CARDNUM
031B	031E	CFLD	DC C4	COMMAND FIELD	744
031C	0323		DC C5	FIELD 1	745
031D	0326		DC C6	FIELD 2	746
031E	E01E	C4	LDR R,CMD,CADD	ADDRESS OF COMMAND	747
0320	4PF8	C7	ADD IS,CINDX,1	INCREMENT PATH INDEX	748
0321	C107		LDR LDR IS,CFIG,-1	SET FLAG FOR IN ENTRY	749
0322	E01F	C5	BRCL U,C3	KEEP GOING	750
0323	C10F		LDR R,CF1,CADD	ADDRESS OF FIELD 1	751
0324	C107	C6	BRCL U,C7	KEEP GOING	752
0326	E019		LDR R,CF2,CADD	ADDRESS OF FIELD 2	753
0327	200F	C6A	CMP IS,CP1,0	SEE IF FIELD 1 IS PRESENT	754
0328	C102		BRCL EQ,C8	GO PROCESS COMMAND ONLY	755
032A	E0F1		CONVERT FIELD 1 TO HEX		756
032B	E000		LDR R,CADD,CP1	PUT ADDRESS IN REGISTER	757
032D	E02F		BAL I,RET,AXEX	CONVERT VALUE	758
032E	2009		LDR R,CF1,CA1	PUT HEX VALUE IN FIELD	759
032F	C102		CMP IS,CF2,0	SEE IF FIELD 2 IS PRESENT	760
0331	E091		BRCL EQ,C8	GO PROCESS COMMAND	761
0332	E000		CONVERT FIELD 2 TO HEX		762
0334	E029		LDR R,CADD,CF2	PUT ADDRESS IN REGISTER	763
0335			BAL I,RET,AXEX	CONVERT VALUE	764
0336			LDR R,CF2,CA1	PUT HEX VALUE IN FIELD	765
0337			BRANCH TO PROCESS ON COMMAND		766
0338			C8		767
0339	5PAC		LDR RX,CV1,CZERO,CMD	GET FIRST CHARACTER OF COMMAND	768
0340	601E		ADD IS,CMD,1	INCREMENT ADDRESS	769
0341	5PAD		LDR RX,CV2,CZERO,CMD	GET SECOND CHARACTER OF COMMAND	770
0342	A10D		AND I,CV2,000FF	CLEAR UPPER BITS	771
0343	A87C		SUB I,CV1,8	LEFT JUSTIFY 1ST CHARACTER	772
0344	80DC		ADD R,CV1,CV2	PUT 1ST 2 CHARACTERS IN ONE WORD	773
0345	B10C		CMP I,CV1,0646F	COMPARE WITH 'DO'	774
0346	C102		BRCL EQ,C9	GO PROCESS DONE	775
0347	B10C		CMP I,CV1,06475	COMPARE WITH 'DU'	776
0348	C102		BRCL EQ,C10	GO PROCESS DUMP	777
0349	B10C		CMP I,CV1,06469	COMPARE WITH 'DI'	778
0350	C102		BRCL EQ,C11	GO PROCESS DISPLAY	779
0351	B10C		CMP I,CV1,06368	COMPARE WITH 'CH'	780

ATAC	LOC	OBJECT CODE	CARD IMAGE	TIME: 15:22:49	03/21/77	PAGE	CARDNUM
034A	C102 039C	BRCL	EQ,C12	GO PROCESS 'CHANGE'			797
034C	B10C 6373	CMP	I,CV1,06373	COMPARE WITH 'CS'			798
034E	C102 03A0	BRCL	EQ,C20	GO PROCESS CHANGE SEQUENTIAL			799
0350	C107 02FD	BRCL	U,C1	INVALID COMMAND, GO TRY AGAIN			800
							801
							802
							803
							804
							805
							806
							807
							808
							809
							810
							811
							812
							813
							814
							815
							816
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0377	6FF1	03F1	IS, CADD, -1	DECREMENT BY ONE TO GET COUNT	850
0378	9CF0	0230	D, O, CS1, 16	SAVE REGISTERS	851
037A	ED00	0230	I, RET, OUTPUT	OUTPUT ONE LINE	852
037C	BCF0	03F1	D, O, CS1, 16	RESTORE REGISTERS	853
037E	6FF7		IS, CINDX, -1	DECREMENT LINE COUNTER	854
037F	C105	035A	NZ, C13	DO ANOTHER LINE	855
0381	C107	02FD	I, 7, C1	WAIT FOR ANOTHER COMMAND	856
			BRC		857
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0383	E0F1	02BB	R, CADD, CFI	GET ADD OF LOCATION TO DISPLAY	
0384	ED00	02BB	I, RET, HEXA	CONVERT CORE CONTENTS TO ASCII	
0386	9C02	040A	D, CA2, CBUD1, 1	PUT MSD IN OUTPUT BUFFER	
0388	E3F1	0000	D, CA2, CBUD1, 1	PUT LSD IN OUTPUT BUFFER	
038C	ED00	02BB	I, RET, HEXA	PUT CORE VALUES IN REGISTER	
038E	9C02	040D	D, CA1, CBUD2, 1	CONVERT ADDRESS TO ASCII	
0390	9C03	040E	I, CADD, CBUD	PUT MSD IN OUTPUT BUFFER	
0392	E101	0409	I, RET, OUTPUT	PUT LSD IN OUTPUT BUFFER	
0394	ED00	0230	D, CA2, CBUD2, 1	PUT ADDRESS IN REGISTER	
0396	E20F	0412	I, RET, OUTPUT	OUTPUT BUFFER TO CRT	
0398	C105	03C5	D, CFI, CSPLG	GET FLAG FOR SEQUENTIAL CHANGE SET	
039A	C107	02FD	I, 7, C1	GO BACK TO SEQUENTIAL IF FLAG SET	
			BRC	GO AGAIN	

039C	9BF9	0000	DX, CF2, 0, CFI	CHANGE CORE CONTENTS	
039E	C107	03B3	I, 7, C1	GO DISPLAY CORE CHANGE	

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ATAC  
LOC

OBJECT CODE

CARD IMAGE

\*\*\*\*\*  
: CHANGE CORE SEQUENTIALLY  
: \*\*\*\*\*

03A0 9C0F 0410 STR D,CPI,CSTRT  
03A2 9C0F 0411 STR D,CPI,CSTRT  
03A4 401C 0412 LDR D,CV1,CSTRT  
03A5 9C0C 0412 STR D,CV1,CSTRT  
03A7 4000 0415 BAL D,CV1,CSTRT  
03A9 4000 0415 LDR D,CV1,CSTRT  
03AA 6011 ADD D,CV1,CSTRT  
03AB 4015 LDR D,CV1,CSTRT  
03AC 51AC LDR D,CV1,CSTRT  
03AD 51AD LDR D,CV1,CSTRT  
03AE AE7C SHS LL,CV1,8  
03AF AE7C SHS LL,CV1,8  
03B0 AD7D ADD R,CV1,CV2  
03B1 80DC CMP R,CV1,CV2  
03B2 B10C BRCL R,CV1,CV2  
03B4 E20F 0411 LDR D,CV1,CSTRT  
03B6 E20F 0411 LDR D,CV1,CSTRT  
03B8 9BF2 0000 STR D,CV1,CSTRT  
03BC 601F 0411 STR D,CV1,CSTRT  
03BD 9C0F 0411 STR D,CV1,CSTRT  
03BE C107 0411 LDR D,CV1,CSTRT  
03BF E20F 0410 LDR D,CV1,CSTRT  
03C1 C107 0410 LDR D,CV1,CSTRT  
03C3 C107 0410 LDR D,CV1,CSTRT  
03C5 E20C 0410 LDR D,CV1,CSTRT  
03C7 601C ADD D,CV1,CSTRT  
03C8 9C0C 0410 STR D,CV1,CSTRT  
03CA E20C 0411 LDR D,CV1,CSTRT  
03CC C104 0411 LDR D,CV1,CSTRT  
03CE 400C 0412 LDR D,CV1,CSTRT  
03CF 9C0C 0412 BRCL D,CV1,CSTRT  
03D1 C107 02FD BRCL D,CV1,CSTRT

\*\*\*\*\*  
: DATA AND BUFFERS  
: \*\*\*\*\*

03D3 CSAVE DS 1  
03D4 001C CBCNT DC 28  
03D5 000A CBUFP DS 27  
03F0 000A DC 0000A

ADDRESS OF ROUTINE CALLING CORE

COUNT OF VALUES IN BUFFER TO OUTPUT  
OUTPUT BUFFER  
CR/LF

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REG SAVE AREA FOR INTERNAL USE

CARD IMAGE

OBJECT CODE

ATAC

CARDNUM

REG SAVE AREA FOR INTERNAL USE

CARD IMAGE

OBJECT CODE

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CARDNUM

REG SAVE AREA FOR INTERNAL USE

CARD IMAGE

OBJECT CODE

ATAC

ATAC  
DS 0500  
ENTRY WJ

RET EQU 0  
OUTPUT EQU 00230  
KEYHR EQU 00151

\*\*\*\*\*  
ESTABLISH EQUATES  
\*\*\*\*\*

WJXS EQU 1  
WJXE EQU 2  
WJX1 EQU 3  
WJX2 EQU 4  
WJX3 EQU 5  
WJX4 EQU 6  
WJD1 EQU 7  
WJD2 EQU 8  
WJD3 EQU 9  
WJD4 EQU 10  
WJYX EQU 11  
WJV1 EQU 1  
WJV2 EQU 2  
WJV3 EQU 3  
WJV4 EQU 4  
WJV5 EQU 5  
WJV6 EQU 6  
WJV7 EQU 7  
WJV8 EQU 8  
WJV9 EQU 9  
WJV10 EQU 10  
WJV11 EQU 11  
WJLPC EQU 15

\*\*\*\*  
ENTRY  
\*\*\*\*

WJ STR D,RET,WJRET

\*\*\*\*\*  
INITIALIZE RECEIVER  
\*\*\*\*\*

WJ01 LDRM D,WJV1,WJL1,4  
STRM D,WJV1,WJCD,8  
LDRM D,WJV1,WJCD,8  
STRM D,WJV1,WJCD,8

SAVE RETURN ADDRESS

GET INITIAL CONTROL WORDS FOR RCVR  
PUT INITIAL VALUES INTO CONTROL  
GET INITIAL CONTROL WORD DISPLAY  
SAVE INITIAL CONTROL WORD DISPLAY

XAR START  
XAR END  
XAR 1  
XAR 2  
XAR 3  
XAR 4  
DATA 1  
DATA 2  
DATA 3  
DATA 4  
XAR FOR CHECK  
VARIABLE 1  
VARIABLE 2  
VARIABLE 3  
VARIABLE 4  
VARIABLE 5  
VARIABLE 6  
VARIABLE 7  
VARIABLE 8  
VARIABLE 9  
VARIABLE 10  
VARIABLE 11  
WJS COUNTER



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ATAC

CEJECT CODE

CARD IMAGE

LOAD "ADDRESS ON"

CARDNUM

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ATAC

CEJECT CODE

CARD IMAGE

LOAD "ADDRESS ON"

CARDNUM

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NAVAL POSTGRADUATE SCHOOL MONTEREY CALIF  
AN INTERACTIVE COMPUTER INTERFACE WITH A DIGITAL RECEIVER.(U)  
MAR 77 W G BORRIES

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2 OF 2  
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03/18/77

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CARD IMAGE

ATAC  
IOC OBJECT CODE

\*\*\*\*\*  
: DISPLAY CONTROL WORD (COMMAND=2)  
: \*\*\*\*\*

WJ30  
E202 09D9 LDR D,WJ2,WJCFU  
E201 09D8 LDR D,WJ1,WJCFU  
E200 07D9 BAL I,RET,WJ92  
E201 09D9 LDR D,WJ1,WJCGM  
E200 0801 LDR D,WJ2,WJCFU  
E201 09D8 BAL I,RET,WJ93  
E200 0820 LDR D,WJ1,WJCGM  
E201 09D8 LDR D,WJ2,WJCFU  
E200 0820 BAL I,RET,WJ94  
E201 09D8 LDR D,WJ1,WJCFU  
E200 084A BAL I,RET,WJ95  
C107 0519 BRCL U,WJ02  
05C6  
05C8  
05CA  
05CC  
05CE  
05D0  
05E2  
05E4  
05E6  
05E8  
05FA  
05DC

GET UPPER OF CONTROL FREQUENCY  
GET LOWER OF CONTROL FREQUENCY  
OUTPUT FREQUENCY  
GET CONTROL IF BANDWIDTH  
GET CONTROL IF BANDWIDTH  
OUTPUT GAIN MODE AND IF BANDWIDTH  
GET CONTROL DETECT MODE  
GET CONTROL BFO FREQUENCY (LOWER)  
OUTPUT DETECT MODE AND BFO FREQUENCY  
GET CONTROL RF GAIN  
OUTPUT RF GAIN  
DONE

\*\*\*\*\*  
: DISPLAY RECEIVED WORD (COMMAND=3)  
: \*\*\*\*\*

WJ40  
E202 09E1 LDR D,WJ2,WJRFU  
E201 09E0 LDR D,WJ1,WJRFU  
E200 07D9 BAL I,RET,WJ92  
E201 09E5 LDR D,WJ1,WJRCM  
E200 09E7 LDR D,WJ2,WJRFU  
E201 0801 LDR D,WJ1,WJRCM  
E200 09E2 LDR D,WJ2,WJRFU  
E201 0820 LDR D,WJ1,WJRCM  
E200 084A LDR D,WJ2,WJRFU  
E201 09E9 LDR D,WJ1,WJRSS  
E200 4002 LDR D,WJ2,0  
E201 2030 SHD LL,WJ1,8  
E200 0822 LDR D,WJ2,02030  
E201 3030 LDR D,WJ2,WJDS1  
E200 4002 LDR D,WJ2,0  
E201 3030 SHD LL,WJ2,4  
E200 4002 SHD LL,WJ2,4  
E201 3030 LDR D,WJ2,03030  
E200 4002 LDR D,WJ2,WJDS1+1  
E201 0818 LDR I,WJ1,WJDS  
E200 0230 BAL I,RET,OUTPUT  
C107 0519 BRCL U,WJ02  
05E0  
05E2  
05E4  
05E6  
05E8  
05EA  
05EC  
05EE  
05F0  
05F2  
05F4  
05F6  
05F8  
05FA  
05FC  
05FE  
05FF  
0600  
0602  
0604  
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060A

GET UPPER OF RECEIVED FREQUENCY  
GET LOWER OF RECEIVED FREQUENCY  
OUTPUT FREQUENCY  
GET RECEIVED IF BANDWIDTH  
GET RECEIVED IF BANDWIDTH  
OUTPUT GAIN MODE AND IF BANDWIDTH  
GET RECEIVED DETECT MODE  
GET RECEIVED BFO FREQUENCY (LOWER)  
OUTPUT DETECT MODE AND BFO FREQUENCY  
GET RECEIVED RF GAIN  
OUTPUT RF GAIN  
GET RECEIVED SIGNAL STRENGTH  
CLEAR REGISTER  
POSITION 1ST DIGIT  
CONVERT TO ASCII  
STORE IN OUTPUT BUFFER  
CLEAR REGISTER 2 DIGITS  
POSITION LAST 2 DIGITS  
CONVERT TO ASCII  
STORE IN OUTPUT BUFFER  
GET ADDRESS OF BUFFER TO OUTPUT  
OUTPUT BUFFER  
DONE  
SPACE FOR PATCHES

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0614	BC71	09D0	LDHM	D,MJV1,MJFEL,8	GET TENTATIVE VALUES IN DISPLAY FORM	267
0616	9C71	09D8	STHM	D,MJV1,MJFEL,8	STORE IN CONTROL VALUES IN DISPLAY FORM	268
0618	9B31		SHD	LL,MJV1,MJCH1	POSITION FREQUENCY	269
0619	9C02	09C8	STR	LL,MJV2,MJCH1	SET UP CONTROL WORD 1	270
061B	AE16		SHS	LL,MJV2,MJCH1	POSITION GAIN MODE	271
061C	A461		IOR	R,MJV2,MJCH1	PUT IN CM 2	272
061D	F082		IDR	R,MJV2,MJCH1	GET IF BANDWIDTH	273
061E	A471		SHS	LL,MJV2,MJCH1	POSITION BANDWIDTH	274
061F	A471		SHS	LL,MJV2,MJCH1	PUT IN CM 2	275
0620	9C01	09C9	STR	D,MJV1,MJCH2	STORE IN CONTROL WORD 2	276
0622	F081		IDR	R,MJV1,MJCH2	GET IF BANDWIDTH	277
0623	AE81		SHS	LL,MJV1,MJCH2	POSITION LAST DIGIT OF BANDWIDTH	278
0624	AE81		SHS	LL,MJV1,MJCH2	POSITION DETECT MODE	279
0625	A431		IOR	R,MJV1,MJCH2	PUT DETECT MODE IN CM 3	280
0626	9C01	09CA	STR	D,MJV1,MJCH3	SAVE CM 3	281
0628	F042		IDR	R,MJV1,MJCH3	GET BFO LOWER VALUE	282
0629	E000	098E	LDR	R,MJV2,MJCH4	CONVERT BCD VALUE TO HEX	283
062B	E501	1194	BAL	I,RET,MJBCDH	SUBTRACT 4500 FROM VALUE	284
062D	CD01	07FF	SUB	I,MJV1,07FF	MULTIPLY BY 7FF	285
062F	E103	07D0	MUL	I,MJV3,2000	SET UP DIVISOR	286
0631	FC31	0373	ADD	I,MJV1,0373	ROUND	287
0633	FC31		DIV	R,MJV1,MJV3	DIVIDE	288
0634	E023		IDR	R,MJV3,MJV2	GET RANGE OF CM 3	289
0635	F201	09CA	LDR	D,MJV1,MJCH3	GET REST OF CM 3	290
0637	A431		IOR	R,MJV1,MJCH3	STORE FREQUENCY INTO CM 3	291
0638	9C01	09CA	STR	D,MJV1,MJCH3	STORE CONTROL WORD 3	292
063A	E202	09D6	IDR	R,MJV1,MJCH3	GET BFO FREQUENCY	293
063C	E000	098E	BAL	I,RET,MJBCDH	CONVERT BCD TO HEX	294
063E	CD01	007F	MUL	I,MJV1,007F	MULTIPLY BY 7F	295
0640	9C21		ADD	IS,MJV1,032	ROUND UP DIVISOR	296
0641	9C21		ADD	IS,MJV1,032	ROUND UP DIVISOR	297
0642	FC31		IDR	R,MJV3,MJV2	DIVIDE	298
0643	N421		LLC	R,MJV1,MJV2	GET VALUE COMPLEMENTED FOR MJ	299
0644	A171	007F	AND	I,MJV1,07F	CLEAR ALL BUT VALUE WANTED	300
0646	5C01	09CB	SHS	LL,MJV1,8	POSITION RE GAIN	301
0647	5C01	09CB	SHS	LL,MJV1,8	POSITION RE GAIN	302
0649	E000	09AE	STR	D,MJV1,MJCH4	STORE CONTROL WORD 4	303
064B	C107	0519	BAL	I,RET,MJJS	OUTPUT CONTROL WORD TO MJ	304
064D			DS	U,MJ02	DONE	305
					SPACE FOR PATCHES	306
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CLEAR REGISTER

\*\*\*\*\*  
: ENTER TENTATIVE CONTROL WORD (COMMAND=4)  
: \*\*\*\*\*

WJ50 LDR IS,MJV1,0

0657 4001

WJ60





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ATAC

LOC	OBJECT CODE	CARD IMAGE	OUTPUT TITLE AND GET SIGNAL STRENGTH	GET ADDRESS OF SIGNAL STRENGTH TITLE	CARDNUM
06CB	E101 09EB	LDR	I.WJV1.WJSSS	GET ADDRESS OF SIGNAL STRENGTH TITLE	373
06CD	E100 07AE	BAL	I.WJV1.WJSSS	OUTPUT TITLE AND GET ENTRY	374
06CF	C107 06CB	BCL	D.WJV6.WJSSFLU	ILLEGAL ENTRY AND GET ENTRY	375
06D1	B103 0100	CHP	I.WJV3.WJSSFLU	COMPARE WITH MAX VALUE	376
06D3	C101 06CB	BCL	G.WJV6.WJSSFLU	ILLEGAL - TOO LARGE MAX	377
06D5	2032	CHP	I.WJV3.WJSSFLU	COMPARE COUNT WITH MAX	378
06D6	C101 06CB	BCL	G.WJV6.WJSSFLU	ILLEGAL - TOO LARGE	379
06D8	E032	LDR	R.WJV2.WJSSFLU	PUT SIGNAL STRENGTH IN REG 2	380
06D9	E000 098E	BAL	I.WJV1.WJSSFLU	CONVERT BCD TO HEX	381
06DB	CD01 007F	MUL	I.WJV1.WJSSFLU	MULTIPLY BY 127	382
06DD	6321	ADD	I.WJV1.WJSSFLU	ROUND	383
06DE	FC31	LDR	I.WJV1.WJSSFLU	SET UP DIVISOR	384
06DF	4643	LDR	I.WJV1.WJSSFLU	DIVIDE BY 100	385
06E0	A102 007F	DIV	I.WJV1.WJSSFLU	CLEAR ALL BUT VALUE WANTED	386
06E2	9C02 09EF	AND	I.WJV2.WJSSFLU	STORE DESIRED SIGNAL STRENGTH	387
06E4		STR	D.WJV2.WJSSFLU	SPACE FOR PATCHES	388
		DS	10		389
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ATAC	LOC	OBJECT CODE	CARD IMAGE	TIME: 16:43:42 03/18/77	PAGE	CARDNUM
072C	E201 09EB	LDR	D.WJV1.WJSPUL	GET UPPER LIMIT (LOWER)	426	
072E	E202 09EA	LDR	D.WJV2.WJSPUL	GET UPPER LIMIT (UPPER)	427	
0730	B062	CMP	K.WJV2.WJVV6	COMPARE UPPER LIMIT AND FREQ (UPPER)	428	
0731	C101 06F2	BRCL	EQ.WJ608	FREQ BELOW LIMIT, KEEP LOOKING	429	
0733	C102 073F	LDR	D.WJV1.WJSCNT	UPPER FREQ MATCH, CHECK LOWERS	430	
0735	E201 09F0	LDR	D.WJV1.WJSCNT	GET COUNT OF NO. OF TIME THRU	431	
0737	6011	ADD	IS.WJV1.1	INCREMENT COUNT	432	
0738	2641	CMP	IS.WJV1.100	COMPARE WITH MAX TIMES THRU	433	
0739	C101 075E	BRCL	IS.WJV1.100	DONE - NO FIND	434	
073B	9C01 09F0	STR	D.WJV1.WJSCNT	SAVE NEW COUNT	435	
073D	C107 06EE	BRCL	U.WJ605	GO START AT LOWER LIMIT AGAIN	436	
073F	B051	CMP	R.WJV1.WJV5	COMPARE LOWERS OP UPPER LIMIT AND FR	437	
0740	C104 0735	BRCL	U.WJ607	LESS GO START AGAIN	438	
0742	C107 06F2	BRCL	U.WJ608	GO DO WITH NEW FREQUENCY	439	
0744		DS	10	SPACE FOR PATCHES	440	
					441	
					442	
					443	
074E	BC11 09E0	LDRM	D.WJV1.WJREFL.2	GET RECEIVED FREQUENCY (DISPLAY)	444	
0750	9C11 09D8	STRM	D.WJV1.WJREFL.2	STORE IN CONTROL FREQ (DISPLAY)	445	
0752	C107 05DE	BRCL	U.WJ40	GO DISPLAY RECEIVED WORD	446	
0754		DS	10	SPACE FOR PATCHES	447	
					448	
					449	
					450	
075E	BC11 09E0	LDRM	D.WJV1.WJREFL.2	GET LAST RECEIVED FREQ (DISPLAY)	451	
0760	9C11 09D8	STRM	D.WJV1.WJREFL.2	STORE IN CONTROL FREQ (DISPLAY)	452	
0762	E101 09CA	LDR	I.WJV1.WJSCNF	GET ADDRESS OF NO FIND MESSAGE	453	
0764	ED00 0230	BAL	I.WJV1.WJSCNF	OUTPUT MESSAGE	454	
0766	C107 0519	BRCL	U.WJ02	DONE	455	
0768		DS	40	SPACE FOR PATCHES	456	
					457	
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					462	
					463	
0790	E101 0001	LDR	I.WJV1.01	LOAD FLAG TO INHIBIT COMPARE	464	
0792	9C01 09F4	STR	D.WJV1.CHKFLG1	STORE FLAG	465	
0794	ED00 08E1	BAL	I.WJV1.WJR	INPUT RECEIVER CONTROL WORDS	466	
0796	E101 0000	LDR	I.WJV1.0	ZERO REGISTER	467	
0798	9C01 09F4	STR	D.WJV1.CHKFLG1	CLEAR FLAG	468	
079A	C107 05DE	BRCL	U.WJ40	DISPLAY RECEIVED WORDS	469	
079C	C107 0519	BRCL	U.WJ02	RETURN	470	
079E		DS	10	SPACE FOR PATCHES	471	
					472	
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ATAC LOC OBJECT CODE CARD IMAGE

0833 4002 LDR IS,WJV2,0  
 0834 F831 SHD LL,WJV1,4  
 0835 AE32 SHS LL,WJV2,4  
 0836 F831 IOR LL,WJV1,63030  
 0837 3030 STR D,WJV2,WJDBF1  
 0838 0AF5 LDR JS,WJV2,0  
 0839 4002 SHD LL,WJV1,4  
 083C F831 SHS LL,WJV2,4  
 083D AE32 SHD LL,WJV1,63030  
 083E F831 IOR D,WJV2,WJDBF1+1  
 083F 3030 STR D,WJV2,WJDBF1+1  
 0840 0AF6 LDR I,WJV1,WJDBF  
 0841 9C02 BAL I,RET,OUTPUT  
 0842 E101 LDR D,RET,WJ90R  
 0843 0AEE LDR R,7,RET  
 0845 E100 BRC  
 0846 E200  
 0847 09F1  
 0849 BF07

0838 CLEAR REGISTER  
 0839 POSITION UPPER 2 DIGITS  
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CARD IMAGE

OBJECT CODE

ATAC  
IOC

ATAC IOC	OBJECT CODE	CARD IMAGE	SAVE RETURN ADDRESS SET UP MASK CLEAR REGISTER DO 1ST DIGIT DO 2ND DIGIT DO 3RD DIGIT DO 4TH DIGIT DO 5TH DIGIT DO 6TH DIGIT DO 7TH DIGIT	PAGE CARDNUM
0861	9C00	STR	D RET, WJ90R	691
0863	E109	LDR	I, WJ95, 0000F	692
0865	4006	LDR	I, WJ95, 0	693
0866	4006	LDR	I, WJ95, 0	694
0867	E038	LDR	R, WJ95, WJ91	695
0868	E038	LDR	R, WJ95, WJ91	696
0869	E000	BAL	I, RET, WJ961	697
086A	E017	LDR	R, WJ95, WJ91	698
086B	E017	LDR	R, WJ95, WJ91	699
086C	E037	SHS	R, WJ95, 4	700
086D	E037	SHS	R, WJ95, WJ91	701
086E	E038	LDR	R, WJ95, WJ91	702
086F	E038	SHS	R, WJ95, WJ91	703
0870	AD38	BAL	I, RET, WJ961	704
0871	E000	SHS	I, WJ95, 4	705
0873	AE37	SHS	R, WJ95, WJ91	706
0874	A475	LDR	R, WJ95, WJ91	707
0875	E017	LDR	R, WJ95, WJ91	708
0876	AD77	SHS	R, WJ95, WJ91	709
0877	E087	SHS	R, WJ95, WJ91	710
0878	E038	LDR	R, WJ95, WJ91	711
0879	AD78	SHS	R, WJ95, WJ91	712
087A	E000	BAL	I, RET, WJ961	713
087C	AE77	SHS	I, WJ95, 8	714
087D	E017	LDR	R, WJ95, WJ91	715
087E	E017	LDR	R, WJ95, WJ91	716
087F	AD87	SHS	R, WJ95, WJ91	717
0880	E087	SHS	R, WJ95, WJ91	718
0881	E038	LDR	R, WJ95, WJ91	719
0882	AD88	SHS	R, WJ95, WJ91	720
0883	E000	BAL	I, RET, WJ961	721
0885	AE77	SHS	I, WJ95, 12	722
0886	A475	LDR	R, WJ95, WJ91	723
0887	E027	LDR	R, WJ95, WJ91	724
0888	E087	SHS	R, WJ95, WJ91	725
0889	E048	SHS	R, WJ95, WJ91	726
088A	E000	BAL	I, RET, WJ961	727
088C	E076	LDR	R, WJ95, WJ91	728
088D	E027	LDR	R, WJ95, WJ91	729
088E	AD37	SHS	R, WJ95, WJ91	730
088F	E087	SHS	R, WJ95, WJ91	731
0890	E048	SHS	R, WJ95, WJ91	732
0891	AD38	LDR	R, WJ95, WJ91	733
0892	E000	BAL	I, RET, WJ961	734
0894	AE37	SHS	I, WJ95, 4	735
0895	A476	LDR	R, WJ95, WJ91	736
0896	E027	LDR	R, WJ95, WJ91	737
0897	AD77	SHS	R, WJ95, WJ91	738
0898	E087	SHS	R, WJ95, WJ91	739
0899	E048	LDR	R, WJ95, WJ91	740
089A	AD78	SHS	R, WJ95, WJ91	741
089B	E000	BAL	I, RET, WJ961	742
089D	AE77	SHS	I, WJ95, 8	743

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089E 0976 IOR R,WJ6,WJ7 744
089F A8B8 SHS R,WJ6,WJ12 745
08A0 A8B6 IOR R,WJ6,WJ12 746
08A1 E200 09F1 IOR R,WJ6,WJ12 747
08A3 BF07 BRC R,WJ6,WJ12 748
08A4 A097 AND R,WJ6,WJ12 749
08A5 A098 AND R,WJ6,WJ12 750
08A6 8087 ADD R,WJ6,WJ12 751
08A7 4008 LDR IS,WJ6,WJ12 752
08A8 20A7 CMP IS,WJ6,WJ12 753
08A9 C104 08AD BRCL IS,WJ6,WJ12 754
08AB 6E67 ADD LT,WJ6,WJ12 755
08AC 4018 LDR IS,WJ6,WJ12 756
08AD BF07 BRC R,WJ6,WJ12 757
08AE 09A2 ILC D,WJ6,WJ12 758
08AF 09B0 ILC D,WJ6,WJ12 759
08B0 09B1 ILC D,WJ6,WJ12 760
08B1 09B2 ILC D,WJ6,WJ12 761
08B2 09B3 ILC D,WJ6,WJ12 762
08B3 09B4 ILC D,WJ6,WJ12 763
08B4 09B5 ILC D,WJ6,WJ12 764
08B5 09B6 ILC D,WJ6,WJ12 765
08B6 09B7 ILC D,WJ6,WJ12 766
08B7 09B8 ILC D,WJ6,WJ12 767
08B8 09B9 ILC D,WJ6,WJ12 768
08B9 09BA ILC D,WJ6,WJ12 769
08BA 09BB ILC D,WJ6,WJ12 770
08BB 09BC ILC D,WJ6,WJ12 771
08BC 09BD ILC D,WJ6,WJ12 772
08BD 09BE ILC D,WJ6,WJ12 773
08BE 09BF ILC D,WJ6,WJ12 774
08BF 09C0 ILC D,WJ6,WJ12 775
08C0 09C1 ILC D,WJ6,WJ12 776
08C1 09C2 ILC D,WJ6,WJ12 777
08C2 09C3 ILC D,WJ6,WJ12 778
08C3 09C4 ILC D,WJ6,WJ12 779
08C4 09C5 ILC D,WJ6,WJ12 780
08C5 09C6 ILC D,WJ6,WJ12 781
08C6 09C7 ILC D,WJ6,WJ12 782
08C7 09C8 ILC D,WJ6,WJ12 783
08C8 09C9 ILC D,WJ6,WJ12 784
08C9 09CA ILC D,WJ6,WJ12 785
08CA 09CB ILC D,WJ6,WJ12 786
08CB 09CC ILC D,WJ6,WJ12 787
08CC 09CD ILC D,WJ6,WJ12 788
08CD 09CE ILC D,WJ6,WJ12 789
08CE 09CF ILC D,WJ6,WJ12 790
08CF 09D0 ILC D,WJ6,WJ12 791
08D0 09D1 ILC D,WJ6,WJ12 792
08D1 09D2 ILC D,WJ6,WJ12 793
08D2 09D3 ILC D,WJ6,WJ12 794
08D3 09D4 ILC D,WJ6,WJ12 795
08D4 09D5 ILC D,WJ6,WJ12 796
08D5 09D6 ILC D,WJ6,WJ12 797
08D6 09D7 ILC D,WJ6,WJ12 798
08D7 09D8 ILC D,WJ6,WJ12 799
08D8 09D9 ILC D,WJ6,WJ12 800
08D9 09DA ILC D,WJ6,WJ12 801
08DA 09DB ILC D,WJ6,WJ12 802
08DB 09DC ILC D,WJ6,WJ12 803
08DC 09DD ILC D,WJ6,WJ12 804
08DD 09DE ILC D,WJ6,WJ12 805
08DE 09DF ILC D,WJ6,WJ12 806
08DF 09E0 ILC D,WJ6,WJ12 807
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08E1 09E2 ILC D,WJ6,WJ12 809
08E2 09E3 ILC D,WJ6,WJ12 810
08E3 09E4 ILC D,WJ6,WJ12 811
08E4 09E5 ILC D,WJ6,WJ12 812
08E5 09E6 ILC D,WJ6,WJ12 813
08E6 09E7 ILC D,WJ6,WJ12 814
08E7 09E8 ILC D,WJ6,WJ12 815
08E8 09E9 ILC D,WJ6,WJ12 816
08E9 09EA ILC D,WJ6,WJ12 817
08EA 09EB ILC D,WJ6,WJ12 818
08EB 09EC ILC D,WJ6,WJ12 819
08EC 09ED ILC D,WJ6,WJ12 820
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08EF 09F0 ILC D,WJ6,WJ12 823
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08F3 09F4 ILC D,WJ6,WJ12 827
08F4 09F5 ILC D,WJ6,WJ12 828
08F5 09F6 ILC D,WJ6,WJ12 829
08F6 09F7 ILC D,WJ6,WJ12 830
08F7 09F8 ILC D,WJ6,WJ12 831
08F8 09F9 ILC D,WJ6,WJ12 832
08F9 09FA ILC D,WJ6,WJ12 833
08FA 09FB ILC D,WJ6,WJ12 834
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090E 090F ILC D,WJ6,WJ12 854
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091B 091C ILC D,WJ6,WJ12 867
091C 091D ILC D,WJ6,WJ12 868
091D 091E ILC D,WJ6,WJ12 869
091E 091F ILC D,WJ6,WJ12 870
091F 0920 ILC D,WJ6,WJ12 871
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0921 0922 ILC D,WJ6,WJ12 873
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0924 0925 ILC D,WJ6,WJ12 876
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0927 0928 ILC D,WJ6,WJ12 879
0928 0929 ILC D,WJ6,WJ12 880
0929 092A ILC D,WJ6,WJ12 881
092A 092B ILC D,WJ6,WJ12 882
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092C 092D ILC D,WJ6,WJ12 884
092D 092E ILC D,WJ6,WJ12 885
092E 092F ILC D,WJ6,WJ12 886
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0939 093A ILC D,WJ6,WJ12 897
093A 093B ILC D,WJ6,WJ12 898
093B 093C ILC D,WJ6,WJ12 899
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0946 0947 ILC D,WJ6,WJ12 910
0947 0948 ILC D,WJ6,WJ12 911
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0954 0955 ILC D,WJ6,WJ12 924
0955 0956 ILC D,WJ6,WJ12 925
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098A 098B ILC D,WJ6,WJ12 978
098B 098C ILC D,WJ6,WJ12 979
098C 098D ILC D,WJ6,WJ12 980
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098E 098F ILC D,WJ6,WJ12 982
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0904 0905 ILC D,WJ6,WJ12 998
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0906 0907 ILC D,WJ6,WJ12 1000

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CARD IMAGE

OBJECT CODE

ATAC

LOC

LOC	OBJECT CODE	CARD IMAGE	ATAC
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0926	A102	AND	
0928	9C01	STR	
092A	9C02	STR	
092C	E201	LDR	
092E	A101	AND	
0930	A101	AND	
0931	9C01	STR	
0933	E201	LDR	
0935	E202	LDR	
0937	F801	SHD	
0938	A102	AND	
093A	9C02	STR	
093C	A101	AND	
093E	9C01	STR	
0941	E101	LDR	
0943	9C01	STR	
0945	E201	LDR	
0947	A101	AND	
0949	A102	AND	
094A	CD01	MUL	
094C	E103	LDR	
094E	8101	ADD	
0950	FC31	DIV	
0951	8102	ADD	
0953	4003	LDR	
0954	40A4	LDR	
0955	FC42	DIV	
0956	E021	LDR	
0957	E032	LDR	
0958	4003	LDR	
0959	FC42	DIV	
095A	AE32	SHS	
095B	A421	LDR	
095C	E032	LDR	
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09C9	WJCM2	DS 1	2	1009
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09IB	WJTL112	DS 1	112	1127
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09KG	WJTL169	DS 1	169	1184
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09KZ	WJTL188	DS 1	188	1203
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09LV	WJTL210	DS 1	210	1225
09LW	WJTL211	DS 1	211	1226
09LX	WJTL212	DS 1		





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0A24	4544	DC	ED	1117
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0A26	343D	DC	4=	1119
0A27	454E	DC	TE	1120
0A28	5220	DC	TE	1121
0A29	5445	DC	TE	1122
0A2A	5445	DC	TE	1123
0A2B	4154	DC	TE	1124
0A2C	4154	DC	TE	1125
0A2D	4956	DC	TE	1126
0A2E	450D	DC	TE	1127
0A2F	4956	DC	TE	1128
0A30	4956	DC	TE	1129
0A31	4956	DC	TE	1130
0A32	4956	DC	TE	1131
0A33	4956	DC	TE	1132
0A34	4956	DC	TE	1133
0A35	4956	DC	TE	1134
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0A39	4956	DC	TE	1138
0A3A	4956	DC	TE	1139
0A3B	4956	DC	TE	1140
0A3C	4956	DC	TE	1141
0A3D	4956	DC	TE	1142
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0A47	4956	DC	TE	1152
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0A52	4956	DC	TE	1163
0A53	4956	DC	TE	1164
0A54	4956	DC	TE	1165
0A55	4956	DC	TE	1166

ATAC	LOC	OBJECT CODE	CARD IMAGE	COUNT	CARDNUM
			GAIN MODE TITLE BUFFER		
			WJGHB		
0A53	0018		DC	GA	1167
0A54	4741		DC	IN	1168
0A55	494E		DC	M	1169
0A56	204D		DC	OD	1170
0A57	4F44		DC	PCR	1171
0A58	450D		DC	LF0	1172
0A59	0A30		DC	=H	1173
0A5A	3D48		DC	OL	1174
0A5B	4F4C		DC	D	1175
0A5C	4420		DC	AG	1176
0A5D	4147		DC	CCR	1177
0A5E	430D		DC	LF2	1178
0A5F	0A32		DC	=H	1179
0A60	3D4E		DC	OR	1180
0A61	4F52		DC	HA	1181
0A62	4C20		DC	L	1182
0A63	4D41		DC	AG	1183
0A64	4147		DC	CCR	1184
0A65	430D		DC	=H	1185
0A66	0A33		DC	LF3	1186
0A67	304D		DC	AN	1187
0A68	414E		DC	UA	1188
0A69	5541		DC	L	1189
0A6A	4C20		DC	CR/LF	1190
0A6B	0D0A		DC	NULL	1191
0A6C	0000		DC		1192
					1193
					1194
					1195
					1196
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1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673
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LC	00D0A
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<b>. DIRECT MODE TITLE BUFFER</b>	
JJDMB	40
DC	04445
DC	05445
DC	04354
DC	0204D
DC	04744
DC	0450D
DC	04A30
LC	03041
DC	0400D
DC	00A31
DC	00A46
LC	0400D
LC	04A32
DC	03042
DC	0484F
DC	02046
DC	04358
DC	04544
DC	00D0A
DC	0333D
LC	04246
DC	04E20
DC	05641
DC	0520D
LC	00A34
DC	03049
DC	05342
DC	00D0A
LC	03000
LC	04C53
LC	0420D
DC	00A36
DC	03A55
LC	03042
DC	0504A
LC	0373D
DC	0414D
DC	0204E
LC	04C20
DC	00D0A
DC	0
<b>. BFO FREQUENCY TITLE BUFFER</b>	
JJMBF	21
DC	04246
DC	04E20

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0.087	0.08B	5445	0000
0.088	0.08C	4354	0000
	0.08D	204D	
	0.08E	4F44	
	0.08F	450D	
	0.090	0A30	
	0.091	3D41	
	0.092	0A31	
	0.093	4D31	
	0.094	3D46	
	0.095	4D2D	
	0.096	0A32	
	0.097	464E	
	0.098	2096	
	0.099	4958	
	0.09A	4544	
	0.09B	0D0A	
	0.09C	0D0A	
	0.09D	333D	
	0.09E	4246	
	0.09F	4F20	
	0.09A	5641	
	0.0A1	E20D	
	0.0A2	0A34	
	0.0A3	3D49	
	0.0A4	3342	
	0.0A5	0D0A	
	0.0A6	353D	
	0.0A7	4C53	
	0.0A8	420D	
	0.0A9	0A36	
	0.0AB	3D55	
	0.0AB	3342	
	0.0AC	0D0A	
	0.0AD	373D	
	0.0AE	414D	
	0.0AF	204E	
	0.0B0	4C20	
	0.0B1	0D0A	
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0.0B4		4246	
0.0B5		4F20	





ATAC	LOC	OBJECT CODE	CARD IMAGE	COUNT
0A05	0007	WJDDH	DC	1326
0A06	4445		DC	1327
0A07	5445		DC	1328
0A08	4354		DC	1329
0A09	204D		DC	1330
0A0A	4F44		DC	1331
0A0B	4520		DC	1332
0A0C	3D20		DC	1333
0A0D	0000		DC	1334
0A0E	000B		DC	1335
0A0F	4246		DC	1336
0A10	4E20		DC	1337
0A11	4E51		DC	1338
0A12	4E51		DC	1339
0A13	203D		DC	1340
0A14	2034		DC	1341
0A15	2020		DC	1342
0A16	2020		DC	1343
0A17	3020		DC	1344
0A18	485A		DC	1345
0A19	0D0A		DC	1346
0A1A	0000		DC	1347
0A1B	0006		DC	1348
0A1C	4741		DC	1349
0A1D	494E		DC	1350
0A1E	204D		DC	1351
0A1F	4F44		DC	1352
0A20	4520		DC	1353
0A21	3D20		DC	1354
0A22	0000		DC	1355
0A23	0008		DC	1356
0A24	4946		DC	1357
0A25	2042		DC	1358
0A26	414E		DC	1359
0A27	4944		DC	1360
0A28	5448		DC	1361
0A29	203D		DC	1362
0A2A	2020		DC	1363
0A2B	0000		DC	1364
0A2C	0009		DC	1365
0A2D	5246		DC	1366
0A2E	2047		DC	1367
0A2F	4149		DC	1368
0A30	4E20		DC	1369
0A31	000B		DC	1370
0A32	4246		DC	1371
0A33	4E20		DC	1372
0A34	4E51		DC	1373
0A35	203D		DC	1374
0A36	2034		DC	1375
0A37	2020		DC	1376
0A38	3020		DC	1377
0A39	485A		DC	1378
0A3A	0D0A		DC	1379
0A3B	0000		DC	1380
0A3C	0006		DC	1381
0A3D	4741		DC	1382
0A3E	494E		DC	1383
0A3F	204D		DC	1384
0A40	4F44		DC	1385
0A41	4520		DC	1386
0A42	3D20		DC	1387
0A43	0000		DC	1388
0A44	0008		DC	1389
0A45	4946		DC	1390
0A46	2042		DC	1391
0A47	414E		DC	1392
0A48	4944		DC	1393
0A49	5448		DC	1394
0A4A	203D		DC	1395
0A4B	2020		DC	1396
0A4C	0000		DC	1397
0A4D	0009		DC	1398
0A4E	5246		DC	1399
0A4F	2047		DC	1400
0A50	4149		DC	1401
0A51	4E20		DC	1402

LOC	OBJECT CODE	CARD IMAGE	STRENGTH TITLE FOR DISPLAY	COUNT	CR/LF	CARDNUM
OB12	3D20	DC	WJDRF1	03D20	XX	1379
OB13	2020	DC		02020	XX	1380
OB14	2020	DC		02020	XX	1381
OB15	2520	DC		02520	XX	1382
OB16	000A	DC		00D0A	CR/LF	1383
OB17	0000	DC		0	NULL	1384
OB18	000D	DC	WJDSS	13	NULL	1385
OB19	5349	DC		05349	NULL	1386
OB1A	474E	DC		0474E	NULL	1387
OB1B	414C	DC		0414C	NULL	1388
OB1C	2053	DC		02053	NULL	1389
OB1D	5452	DC		05452	NULL	1390
OB1E	454E	DC		0454E	NULL	1391
OB1F	4754	DC		04754	NULL	1392
OB20	4820	DC		04820	NULL	1393
OB21	3D20	DC		03D20	NULL	1394
OB22	2020	DC		02020	NULL	1395
OB23	2020	DC		02020	NULL	1396
OB24	2520	DC		02520	NULL	1397
OB25	000A	DC		00D0A	NULL	1398
OB26	0000	DC		0	NULL	1399
OB27	0B2B	LC	WJGMB	WJGMB	CR/LF	1400
OB28	0B32	LC		WJGMB	NULL	1401
OB29	0B34	LC		WJGMB	NULL	1402
OB2A	0B3C	LC		WJGMB	NULL	1403
OB2B	0005	DC	WJGMB	5	HOLD AGC	1404
OB2C	484F	DC		0484F	NOT USED	1405
OB2D	4C44	DC		04C44	NORMAL AGC	1406
OB2E	2041	DC		02041	MANUAL	1407
OB2F	4743	DC		04743	COUNT/HOLD AGC	1408
OB30	000A	DC		00D0A	HO	1409
OB31	0000	DC		0	LD	1410
OB32	FFFF	DC		-1	A	1411
OB33	0000	DC		0	GC	1412
OB34	0006	DC	WJGMB	6	CR/LF	1413
OB35	4E4F	DC		04E4F	NULL	1414
OB36	274D	DC		0274D	NULL	1415
OB37	514C	DC		0514C	NULL	1416
OB38	2041	DC		02041	COUNT/INVALID ENTRY	1417
OB39	4743	DC		04743	NULL	1418
OB3A	000A	DC		00D0A	COUNT/NORMAL AGC	1419
OB3B	0000	DC		0	NO	1420
					RM	1421
					AL	1422
					A	1423
					CC	1424
					CR/LF	1425
					NULL	1426
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						1431

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CARD IMAGE

OBJECT CODE

LOC

LOC	OBJECT CODE	CARD IMAGE	COUNT/MANUAL	CARDNUM
OB3C	0004	WJGM3	4	1432
OB3D	4D41	DC	MA	1433
OB3E	4E55	DC	NU	1434
OB3F	414C	DC	AL	1435
OB40	0D0A	DC	CR/LF	1436
OB41	0000	DC	NULL	1437
OB42	0B47	DC	NULL	1438
OB43	0B49	DC	NULL	1439
OB44	0B4F	DC	NOT USED	1440
OB45	0B55	DC	500KHZ	1441
OB46	0B5B	DC	2KHZ	1442
OB47	FFFF	DC	4KHZ	1443
OB48	0000	DC	8KHZ	1444
OB49	0004	WJIF0	-1	1445
OB4A	3530	DC	COUNT/INVALID ENTRY	1446
OB4B	3020	DC	NULL	1447
OB4C	485A	DC	COUNT/500KHZ	1448
OB4D	0D0A	DC	50	1449
OB4E	0000	DC	0	1450
OB4F	0004	WJIF1	4	1451
OB50	3220	DC	50	1452
OB51	4B48	DC	0	1453
OB52	5A20	DC	HZ	1454
OB53	0D0A	DC	DC/LF	1455
OB54	0000	DC	NULL	1456
OB55	0004	WJIF2	4	1457
OB56	3420	DC	COUNT/2KHZ	1458
OB57	4B48	DC	2	1459
OB58	5A20	DC	KH	1460
OB59	0D0A	DC	2	1461
OB5A	0000	DC	CR/LD	1462
OB5B	0004	WJIF3	4	1463
OB5C	3820	DC	NULL	1464
OB5D	4B48	DC	COUNT/4KHZ	1465
OB5E	5A20	DC	4	1466
OB5F	0D0A	DC	KH	1467
OB60	0000	DC	2	1468
OB61	0B69	WJDN1B	DC	1469
OB62	0004	WJDN1	4	1470
OB63	3820	DC	CR/LF	1471
OB64	4B48	DC	NULL	1472
OB65	5A20	DC	COUNT/8 KHZ	1473
OB66	0D0A	DC	8	1474
OB67	0000	DC	KH	1475
OB68	0004	WJDN1B	DC	1476
OB69	0B69	WJDN1	4	1477
OB70	3820	DC	CR/LF	1478
OB71	4B48	DC	2	1479
OB72	5A20	DC	CR/LF	1480
OB73	0D0A	DC	NULL	1481
OB74	0000	DC	NULL	1482
OB75	0004	WJDN1B	DC	1483
OB76	0B69	WJDN1	4	1484
OB77	3820	DC	COUNT/500KHZ	1485
OB78	4B48	DC	50	1486
OB79	5A20	DC	0	1487
OB80	0D0A	DC	HZ	1488
OB81	0000	DC	DC/LF	1489
OB82	0004	WJDN1B	DC	1490
OB83	0B69	WJDN1	4	1491
OB84	3820	DC	NULL	1492
OB85	4B48	DC	COUNT/500KHZ	1493
OB86	5A20	DC	50	1494
OB87	0D0A	DC	0	1495
OB88	0000	DC	HZ	1496
OB89	0004	WJDN1B	DC	1497
OB90	0B69	WJDN1	4	1498
OB91	3820	DC	DC/LF	1499
OB92	4B48	DC	NULL	1500
OB93	5A20	DC	COUNT/500KHZ	1501
OB94	0D0A	DC	50	1502
OB95	0000	DC	0	1503
OB96	0004	WJDN1B	DC	1504
OB97	0B69	WJDN1	4	1505
OB98	3820	DC	HZ	1506
OB99	4B48	DC	DC/LF	1507
OB00	5A20	DC	NULL	1508
OB01	0D0A	DC	COUNT/500KHZ	1509
OB02	0000	DC	50	1510
OB03	0004	WJDN1B	DC	1511
OB04	0B69	WJDN1	4	1512
OB05	3820	DC	0	1513
OB06	4B48	DC	HZ	1514
OB07	5A20	DC	DC/LF	1515
OB08	0D0A	DC	NULL	1516
OB09	0000	DC	COUNT/500KHZ	1517
OB10	0004	WJDN1B	DC	1518
OB11	0B69	WJDN1	4	1519
OB12	3820	DC	50	1520
OB13	4B48	DC	0	1521
OB14	5A20	DC	HZ	1522
OB15	0D0A	DC	DC/LF	1523
OB16	0000	DC	NULL	1524
OB17	0004	WJDN1B	DC	1525
OB18	0B69	WJDN1	4	1526
OB19	3820	DC	COUNT/500KHZ	1527
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OB21	5A20	DC	0	1529
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OB23	0000	DC	DC/LF	1531
OB24	0004	WJDN1B	DC	1532
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OB26	3820	DC	NULL	1534
OB27	4B48	DC	COUNT/500KHZ	1535
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OB29	0D0A	DC	0	1537
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OB31	0004	WJDN1B	DC	1539
OB32	0B69	WJDN1	4	1540
OB33	3820	DC	DC/LF	1541
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OB35	5A20	DC	COUNT/500KHZ	1543
OB36	0D0A	DC	50	1544
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OB38	0004	WJDN1B	DC	1546
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OB41	4B48	DC	0	1549
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OB43	0D0A	DC	DC/LF	1551
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OB46	0B69	WJDN1	4	1554
OB47	3820	DC	COUNT/500KHZ	1555
OB48	4B48	DC	50	1556
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OB51	0000	DC	DC/LF	1559
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OB56	5A20	DC	2	1564
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OB58	0000	DC	2	1566
OB59	0004	WJDN1B	DC	1567
OB60	0B69	WJDN1	4	1568
OB61	3820	DC	CR/LD	1569
OB62	4B48	DC	NULL	1570
OB63	5A20	DC	COUNT/4KHZ	1571
OB64	0D0A	DC	4	1572
OB65	0000	DC	KH	1573
OB66	0004	WJDN1B	DC	1574
OB67	0B69	WJDN1	4	1575
OB68	3820	DC	COUNT/8 KHZ	1576
OB69	4B48	DC	8	1577
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OB71	0D0A	DC	2	1579
OB72	0000	DC	CR/LF	1580
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OB74	0B69	WJDN1	4	1582
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OB76	4B48	DC	COUNT/8 KHZ	1584
OB77	5A20	DC	8	1585
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OB10	3820	DC	COUNT/8 KHZ	1618
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OB26	5A20	DC	COUNT/4KHZ	1634
OB27	0D0A	DC	4	1635
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OB31	3820	DC	COUNT/4KHZ	1639
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OB35	0000	DC	2	1643
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OB37	0B69	WJDN1	4	1645
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OB39	4B48	DC	COUNT/4KHZ	1647
OB40	5A20	DC	4	1648
OB41	0D0A	DC	KH	1649
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OB43	0004	WJDN1B	DC	1651
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OB45	3820	DC	CR/LF	1653
OB46	4B48	DC	NULL	1654
OB47	5A20	DC	COUNT/4KHZ	1655
OB48	0D0A	DC	4	1656
OB49	0000	DC	KH	1657
OB50	0004	WJDN1B	DC	1658
OB51	0B69	WJDN1	4	1659
OB52	3820	DC	CR/LF	1660
OB53	4B48	DC	NULL	1661
OB54	5A20	DC	COUNT/4KHZ	1662
OB55	0D0A	DC		





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ATAC	LOC	OBJECT CODE	CARD IMAGE	CARDNUM
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	088C	0003	DC 3	1539
	088D	5553	DC 05553	1540
	088E	4220	DC 04220	1541
	088F	000A	DC 0000A	1542
	0890	0000	DC 0	1543
	0891	0004	DC 4	1544
	0892	414D	DC 0414D	1545
	0893	2D4E	DC 02D4E	1546
	0894	4C20	DC 04C20	1547
	0895	0D0A	DC 00D0A	1548
	0896	0000	DC 0	1549
	0897	0003	DC 3	1550
	0898	5143	DC 05143	1551
	0899	414E	DC 0414E	1552
	089A	0D0A	DC 00D0A	1553
	089B	0000	DC 0	1554
	089C	0009	DC 9	1555
	089D	5354	DC 05354	1556
	089E	4152	DC 04152	1557
	089F	5420	DC 05420	1558
	08A0	4652	DC 04652	1559
	08A1	4551	DC 04551	1560
	08A2	2049	DC 02049	1561
	08A3	4E20	DC 04E20	1562
	08A4	485A	DC 0485A	1563
	08A5	0D0A	DC 00D0A	1564
	08A6	0000	DC 0	1565
	08A7	0008	DC 8	1566
	08A8	454E	DC 0454E	1567
	08A9	4420	DC 04420	1568
	08AA	4652	DC 04652	1569
	08AB	4551	DC 04551	1570
	08AC	2049	DC 02049	1571
	08AD	4E20	DC 04E20	1572
	08AE	485A	DC 0485A	1573
	08AF	0D0A	DC 00D0A	1574
	08B0	0000	DC 0	1575
	08B1	000B	DC 11	1576
	08B2	4652	DC 04652	1577
	08B3	4551	DC 04551	1578
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ATAC	LOC	OBJECT CODE	CARD IMAGE	PAGE
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0BE3	5400E	DC	0540E	1645
0BE4	5200E	DC	0520E	1646
0BE5	4100E	DC	0410E	1647
0BE6	4500E	DC	0450E	1648
0BE7	4400E	DC	0440E	1649
0BE8	5200E	DC	0520E	1650
0BE9	5300E	DC	0530E	1651
0BEA	4300E	DC	0430E	1652
0BEB	4900E	DC	0490E	1653
0BEC	4500E	DC	0450E	1654
0BED	C707	DC	00707	1655
0BEE	0D0A	DC	00D0A	1656
0BEF	0000	DC	0000	1657
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